7

Valve Scaling Circuits

The binary circuits described in this chapter are in their zero state when the right-hand valve of each binary is conducting. This does not, however, apply in the case of the ring of binary circuits shown in Fig. 7.7.

Ordinary high vacuum thermionic valves can operate at very high speeds, but it is normally convenient to use them only in binary circuits for counting, either as simple cascaded binaries or as decade counters consisting of groups of four binaries with feedback (see Chapter 1). In decade circuits eight valves per decade are required but, if double triodes are employed, four of the double tubes per decade can be used. It is not easy to use hard valves in ring circuits, since they do not have two characteristic stable states such as those of trigger tubes or four layer diodes.

The space occupied by a valve counting decade is relatively large and the power consumed results in much heat being generated. Resolving times of less than 1 μsec can be obtained with careful circuit design and component layout.

7.1 BINARY COUNTERS

The simple valve bistable circuit is basically that which was first described by Eccles and Jordan in 1919[1]; it has been discussed in Chapter 1. Before the invention of semiconductors and decade tubes, valve binary circuits were the only available means for counting pulses at fairly high speeds. Such circuits were, therefore, much used in nuclear research and radio-isotope work, the most common form of readout being obtained by means of small neon diodes in the valve anode circuits. Valve scaling circuits are still being used in some modern equipment, but as high speed semiconductors become cheaper, they are tending to gradually replace many of the valve circuits, since printed circuit techniques using semiconductors enable very compact apparatus to be constructed.

The two valves in each binary circuit behave as switches which are alternately opened and closed. At any one time one of the two valves in each binary is conducting. Thus two stable states are possible. The conducting valve takes grid current, its grid being at approximately the same potential as the cathode. The grid of the non-conducting valve is driven well beyond cut off. The operating point on the valve characteristics thus moves over a large range and therefore the characteristic cannot be approximated to a straight line. This means that the normal small signal equivalent circuits of the valve cannot be used in circuit design, since the mutual conductance, amplification factor and internal anode resistance vary considerably in value as the operating point moves along the characteristic curve. The detailed analysis of valve binary circuit design, however, has been published elsewhere[2].

7.1.1 Capacitor Coupling

When a binary stage is switched, the pulse produced at the anode of each tube approximates to part of a rectangular wave and is, therefore, suitable for the operation of a succeeding binary stage. A binary

stage may be triggered by the application of successive input pulses of alternating polarity to the grid of one valve, but it is normally much more convenient to apply input pulses of constant polarity to the grids of both valves in the binary. This may be done by means of capacitive coupling as in the circuit of Fig. 7.1 in which two cascaded binary stages are shown. The components C_2R_2 and C_4R_7 effectively differentiate the input pulses before they reach the grids of the first binary.

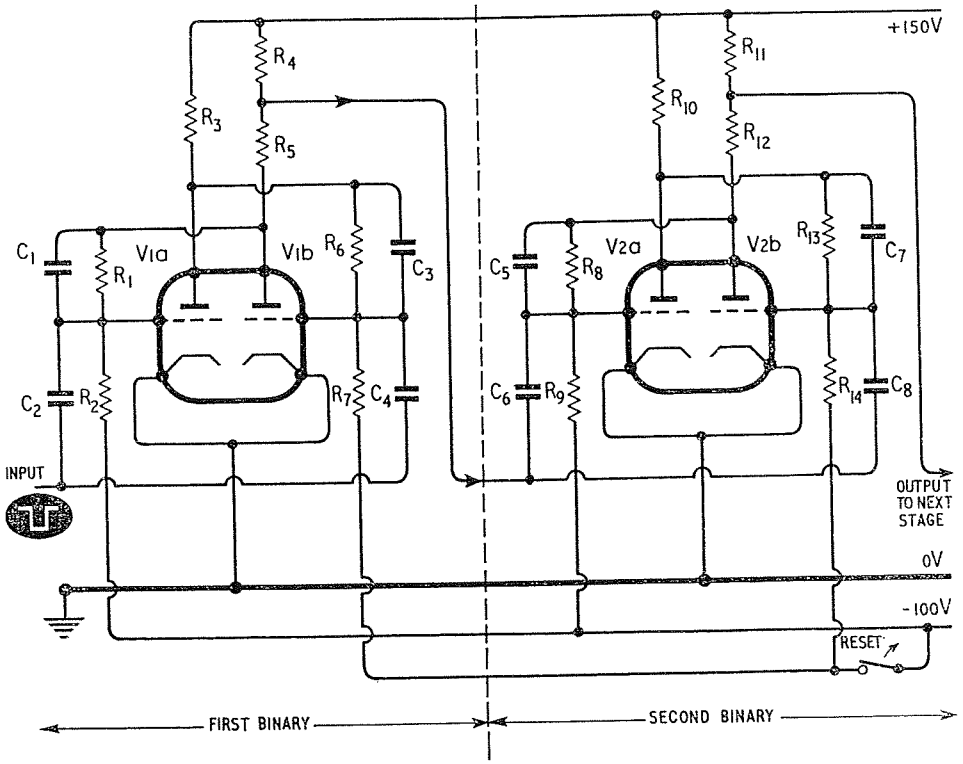


Fig. 7.1 Two cascaded binary circuits

The capacitors C_1 and C_3 are connected across the feedback resistors R_1 and R_6 so that the high frequency components of the waveform at each anode can reach the grid of the other valve in the binary almost unaffected by the stray grid to earth capacitance. If C_1 (or C_3) were omitted, the resistor R_1 (or R_6) and the stray grid capacitance would effectively integrate the high frequency components of the anode waveform. The steep leading edge of the anode waveform would then not reach the grid and this would result in an increased resolving time. C_1 and C_3 should normally be somewhat larger than the input capacitors C_2 and C_4.

The zero state of the circuit occurs when $V1$b and $V2$b are conducting and the other two triodes are cut off. If the circuit is in the zero state and a negative going pulse is applied at the input, the pulse will reach the two grids of the first binary via C_2 and C_4. It will not immediately affect the anode current of $V1$a, since this tube is cut off, but it will reduce the anode current of $V1$b. The anode of $V1$b, therefore, becomes more positive and the positive pulse is fed to the grid of $V1$a via C_1 and R_1. As soon as $V1$a begins to conduct, its anode potential will fall and this results in the grid potential of $V1$b falling also owing to the presence of the coupling components R_6 and C_3. Thus a cumulative effect occurs at the end of which $V1$a is conducting and $V1$b is cut off. The junction of R_4 and R_5 becomes more positive during the switching operation and this positive pulse is coupled to the grids of the second binary stage. It will not appreciably

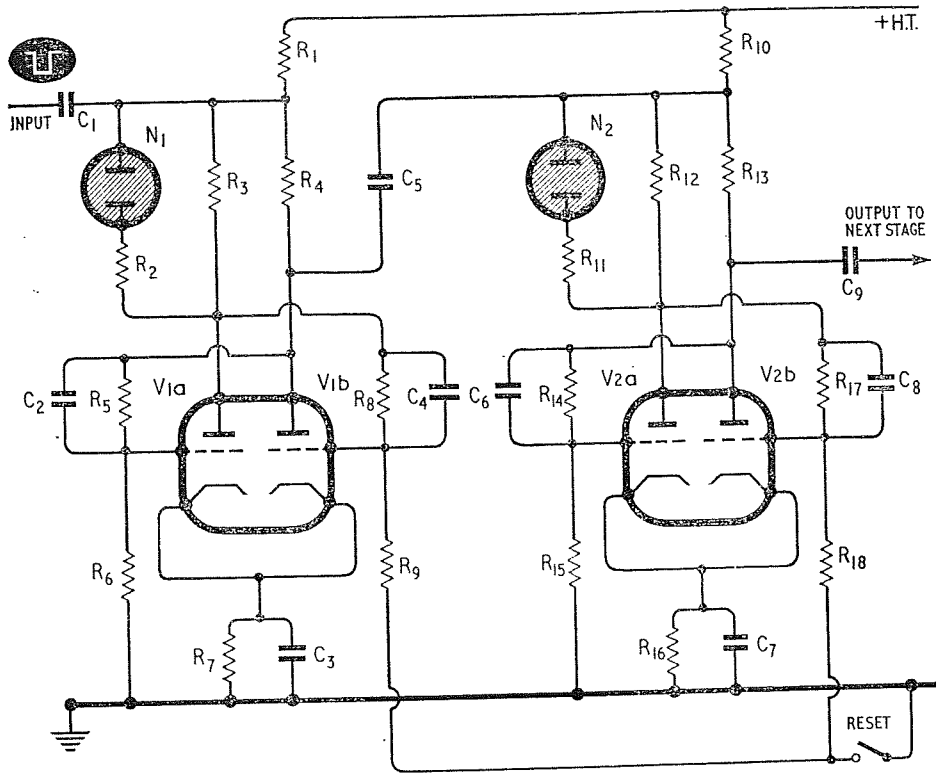


Fig. 7.2 Two cascaded binaries with anode coupling and neon readout

affect the valve which is already conducting (V2b) and is of too small an amplitude to reduce the large negative bias at the grid of V2a to a point at which this tube commences to conduct. Thus the second binary remains in the zero state.

A second negative going pulse applied at the input will cause V1a to return the non-conducting state; that is, the first binary is returned to zero. A negative pulse will be formed at the junction of R_4 and R_5 when V1b conducts and this will have an amplitude which is sufficient to cut off the conducting tube in the second binary, V2b. Thus the second binary is switched at the second input pulse.

The third input pulse switches V1a to the conducting state. The positive pulse formed at the anode of V1b does not affect the second binary. The fourth pulse switches the first binary back to zero and a negative going pulse from the anode circuit of V1b switches the second binary back to zero. The second binary provides a negative going output pulse which can be used to switch a third binary stage.

The capacitors C_2, C_4, C_6 and C_8 in Fig. 7.1 prevent interaction of the two d.c. grid potentials of any stage, block the steady potential from the anode of the previous binary, and convert the pulses into sharp peaks by differentiating them. The reset switch can be used to disconnect the grids of V1b and V2b from the -100 V line. The grid potentials of these tubes will then rise, since the grids are coupled to the anode of the other tube in the binary. Thus the circuit is reset to zero.

The triggering of valve binary stages is almost invariably carried out by the negative edges of the input waveform. This is because the grid voltage of a conducting triode in a bistable circuit is approximately equal to the cathode potential of the tube and the stage can, therefore, be triggered by negative going pulses of a few volts in amplitude. By a suitable choice of component values it can be arranged that the grid of the valve which is cut off is at a potential well below that of the cathode and the positive edges of pulses of a normal amplitude do not, therefore, affect the circuit, since they do not raise

the grid potential of the cut off valve to a value at which anode current commences to flow. Nevertheless, the positive going edges will produce a transient increase in the anode current of the conducting tube. Another reason for the use of negative going edges of pulses for triggering valve bistable circuits is that the negative edges from the anode of a previous binary stage have a greater slope than the positive edges; when they are differentiated by the input capacitors they, therefore, produce pulses of greater amplitude than those produced by the positive going edges. It is possible to use positive going pulses for triggering valve binary stages provided that the negative pulses are removed by diodes but this merely complicates the circuitry and does not have any advantages.

The circuit of Fig. 7.1 can be used to divide the incoming pulse rate by a factor of four, but no form of readout is provided. It would be possible to include meters in series with R_3 and R_{10} so that when $V1$a or $V2$a is conducting, a current is indicated by the corresponding meter. Another form of readout which is more commonly used is shown in Fig. 7.2; it consists of two neon tubes (N_1 and N_2) placed across the anode resistor of the left hand triode of each binary stage. When one of these triodes conducts, the voltage developed across R_3 or R_{12} will cause the corresponding neon tube to glow. When $V1$b and $V2$b are conducting, neither neon is glowing and the count is zero. After the first input pulse N_1 glows, after the second input pulse N_2 only glows, whilst the third input pulse causes both N_1 and N_2 to glow. Both neons are extinguished at the fourth input pulse. Thus the readout is binary in nature.

The bias required for the triodes of Fig. 7.2 is developed across the cathode resistor of each stage. Anode coupling from the first binary to the second occurs via C_5. This method of coupling enables the stray grid capacity to be minimised. If the circuit is first switched to zero by means of the reset switch, $V1$b and $V2$b will conduct. A negative pulse applied at the input will momentarily reduce the potentials of both anodes of the first binary. A part of this potential drop will be communicated to the grids by means of the coupling components. The fall in grid potential will not produce any effect in the non-conducting valve, but it causes the anode current of the conducting valve to fall and initiates the cumulative action which results in the switching of the first binary. The positive pulse produced at the anode of $V2$b is passed to the second binary, but its amplitude is insufficient to cause the stage to switch.

Common anode resistors are used in the circuit of Fig. 7.2. A similar circuit can be designed in which the common resistor is included in the cathode circuit, but in this case positive going pulses capacitively fed to the cathode are required to switch the circuit. The amplification is reduced by the presence of the common cathode resistor and larger values of anode resistor may therefore be required. This results in increased switching time and such circuits are, therefore, not normally used.

7.1.2 Diode Coupling

The resolving time of valve counting circuits may be reduced if diodes are employed as the coupling elements between the binary stages (as shown in Fig. 7.3) instead of the coupling capacitors used in the circuits described previously. In addition, the use of diode coupling is said to reduce the probability of spurious counts being recorded. Suitable semiconductor diodes may be used in place of the thermionic diodes. The cathodes of the first diodes ($V1$ in Fig. 7.3) must receive a suitable positive bias in addition to the negative going input pulses. A suitable potential divider is shown, but the pulses are normally derived from the anode circuit of a valve which also supplies the positive bias.

If the circuit is reset to zero, the right-hand triode of each binary conducts. When a negative going pulse is applied, the upper diode of $V1$ will prevent the pulse from reaching the conducting triode of $V2$, since the anode potential of the conducting triode is less than the positive bias voltage applied to the diode cathodes. The anode of the left-hand triode of $V2$ is, however, at the full H.T. potential, since this valve is not conducting. The lower diode of $V1$ is thus forward biased and the input pulse can pass through it to the anode of the left-hand triode of $V2$. The pulse is coupled to the grid of the right-hand triode which is thus cut off and the stage

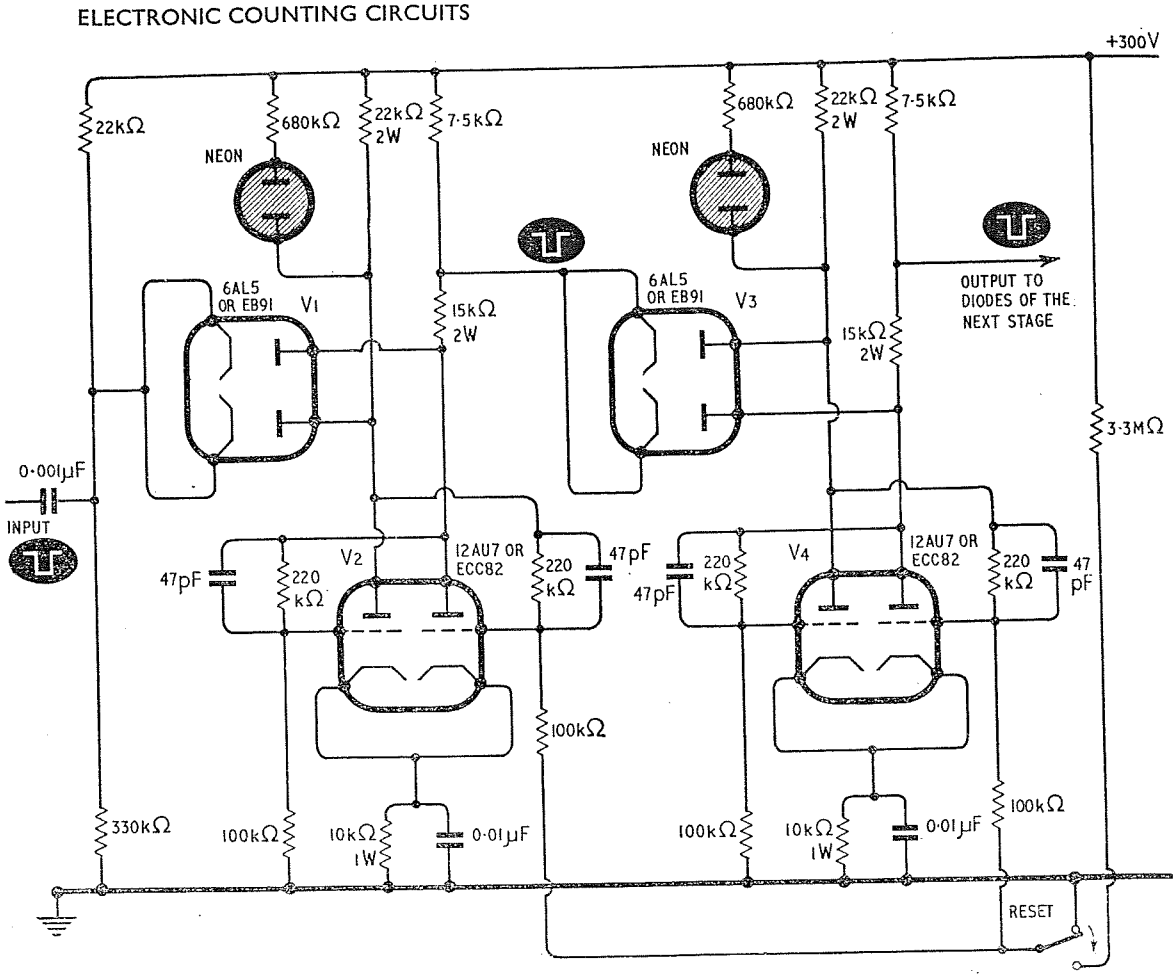


Fig. 7.3 Diode coupling for two cascaded binaries

is switched. The next input pulse will be gated to the anode of the right-hand triode by $V1$. Thus the input diodes route the pulses to the grid of the conducting triode.

The circuit shown in Fig. 7.3 has a resolving time of the order of 5 μsec or less, depending somewhat on the circuit layout. The resistor values in the succeeding stages may be somewhat larger than those shown, since larger time constants are permissible in slower stages. The current consumption of the succeeding stages will then be considerably reduced and less heat will be dissipated.

In any valve bistable circuit it is probably well worth while including grid stopper resistors of between about 50 and 1,000 Ω to prevent spurious oscillations from occurring. Although these oscillations do not interfere with the functioning of a scaler, they may cause appreciable interference with neighbouring V.H.F. radio receivers.

7.1.3 A Valve Decade Using Gating Diodes

The circuit of Fig. 7.4 may be used to show a method in which triodes can be used for decade counting. This circuit is the first decade of the A.E.R.E. 1009E Scaler[3] which has been much used for radioisotope work. The decade shown has a resolving time of about 1 μsec, but the minimum resolving time of the complete scaler is set at 5 μsec. A neon tube will glow when the valve to which it is connected is in the non-conducting state, since the neon tubes are connected across the valves instead of across the anode resistors as in the two circuits discussed previously. They are, therefore, connected

across the right-hand triodes so that they glow when these triodes are non-conducting.

When the reset switch is operated, the triode on the right-hand side of each binary will conduct and no neons will glow. The first negative going input pulse will be routed by the *V*5 diodes to the anode of *V*6a and will then pass through the parallel resistor and capacitor to the grid of *V*6b. *V*31, therefore, ignites.

The second negative going input pulse switches *V*6 back to the zero state and a negative going pulse from the anode of *V*6b is applied to the cathodes of *V*13. The anodes of *V*12b and *V*13*a* are at a fairly low potential, since *V*12*b* is conducting. *V*13a, therefore, prevents the pulse from passing to *V*12b. The pulse can, however, pass through *V*13b to *V*7 and it then switches *V*8. *V*11a is non-conducting, since its cathode is at the H.T. supply potential.

The next few pulses are counted in the normal binary manner, negative going pulses from the *V*6b anode circuit passing through *V*13b and either *V*7a or *V*7b. At the eighth input pulse *V*12 is switched. The potential of the anode of *V*12b now rises to a value equal to that of the H.T. line (since the valve is no longer conducting) and, therefore, the diode *V*13a can pass negative going pulses to the anode of *V*12b. The ninth pulse merely switches *V*6, but at the tenth input pulse the negative pulse occurring in the anode circuit of *V*6b passes through *V*13a to the anode of *V*12b and hence to the grid of *V*12a. *V*12 is, therefore, switched and provides an output pulse to the next decade. The pulse from *V*6b cannot pass through *V*13b to operate *V*8 because the anode current being taken by *V*12a (immediately before *V*12 is switched back to zero) reduces the cathode voltage of *V*11a and this in turn reduces the anode voltage of *V*13b to a point at which the latter is cut off. Soon after *V*12 has returned to the zero state, *V*13b will conduct again and *V*13a will be cut off. All of the binaries are now in their zero state and the circuit is ready to count the next ten inpulses. The binary numbers omitted are ten to fifteen inclusive.

The first binary stage used in Fig. 7.4 takes a current of about 13 mA and can operate at the highest frequency. The component values used in the three succeeding binaries allow a conducting triode to pass about 10 mA. In the 1009E scaler the decade shown is followed by a decade working on similar principles, but employing binary stages which each pass about 5 mA. This economises in current and reduces the heat dissipation, but nevertheless a cooling fan is normally used with a 1009E scaler. The two valve decades are followed by an electro-magnetic counter which limits the maximum continuous counting speed of the scaler (but not the resolving time for a limited number of pulses). This type of scaler may be used at high frequencies if the output from the second valve decade is fed into another scaler of the same type; alternatively a Dekatron add-on unit may be employed[4].

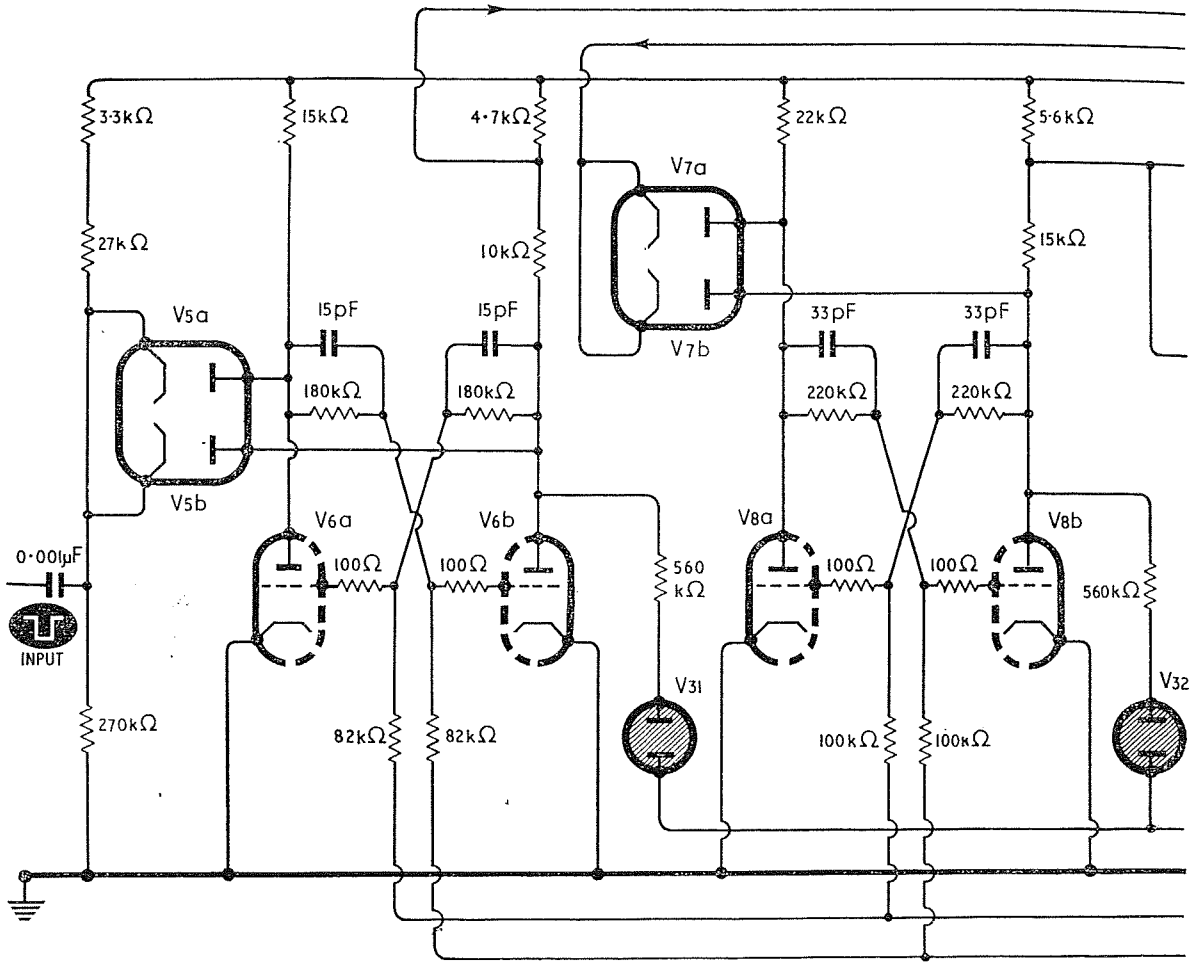
7.1.4 Decade Circuit with GR10A Readout

High speed valve scaling circuits are often followed by simpler but slower cold cathode decade tube counting circuits. In such cases it is desirable to provide a similar visual display of the state of the count in the valve circuits to that provided by the cold cathode decade tubes. This can be achieved by the use of certain indicator tubes such as the GR10A, the Z503M, etc. to provide readout from the valve decades.

A typical circuit of this type is shown in Fig. 7.5, this being the first decade of the Ecko N530F automatic scaler[5]. In this circuit the gating diodes, *V*47, are arranged so that a scale of ten is formed by the omission of the numbers 6, 7, 8, 9, 14 and 15 from the binary scale of 16. The effect of the applied input pulses is as shown in Table 7.1, the binary numbers shown in brackets being possible intermediate states which are included for explanatory purposes only.

When the circuit has been reset, the right hand triode of each of the binaries *V*5, *V*7, *V*9 and *V*11 conducts. The grid of *V*9a is therefore at a pot ential considerably below the cut off potential of this valve and this results in the diode *V*47a being in a non-conducting state, since its anode is connected to the grid of *V*9a. Similarly *V*47b is non-conducting.

The first few pulses are counted in the normal binary manner unaffected by the presence of *V*47. The fourth pulse switches *V*9 and the change in the grid potential of *V*9a renders *V*47a conducting. The

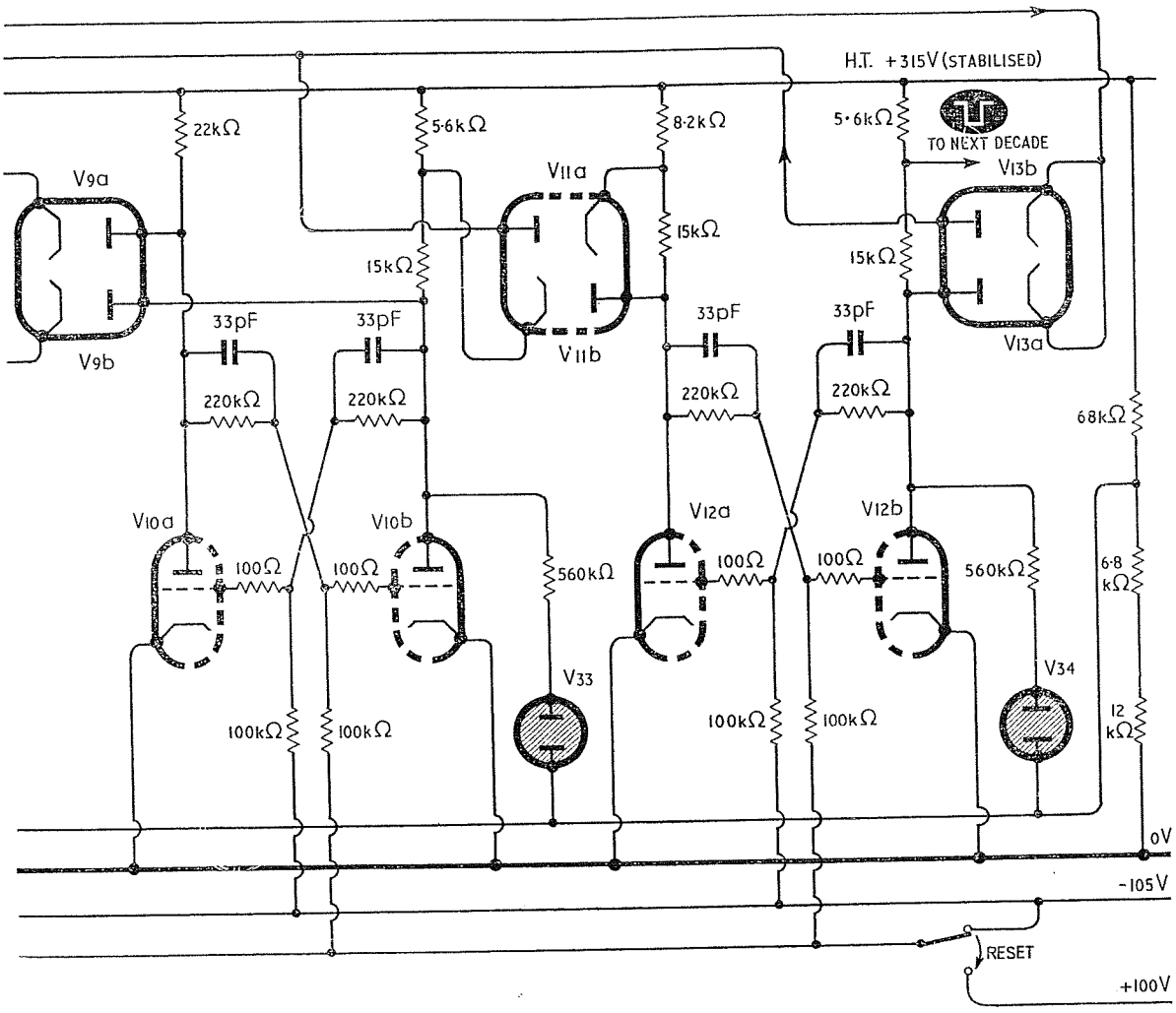


V5 = V7 = V9 = V11 = V13 = CV4007 = 6AL5 = CV140
V6 = V8 = V10 = V12 = CV4031 = M8081 = 6J6 = ECC91 = CV858
V31 = V32 = V33 = V34 = CV2213 = NT2

Fig. 7.4 A valve decade using gating diodes

fifth input pulse merely switches *V*5, since the positive going output pulse from *V*5b cannot pass through either *V*6 or *V*47 from cathode to anode. The sixth input pulse switches *V*5 and the resulting negative going output pulse from *V*5 passes through *V*47a and switches *V*9. In addition the output pulse from *V*5 also passes through *V*6 and switches *V*7. Thus the decade jumps to the binary number 1010 which is ten. *V*9a is now in the cut off state and, therefore, the routing diode *V*47a becomes non-conducting again. The seventh, eighth and ninth input pulses are counted in the normal binary manner, but the eighth pulse switches *V*9 and so allows *V*47a to conduct. The tenth pulse switches *V*5 back to zero and the output pulse from *V*5b passes through *V*47a to switch *V*9 to zero and also through *V*6 to switch *V*7 so that the latter indicates a count. The output pulse from *V*9 switches *V*11 to zero and a pulse from the anode of *V*11b is passed back through *V*47b to switch *V*7 to zero. The binaries are at zero and *V*11b has provided a pulse to the next decade.

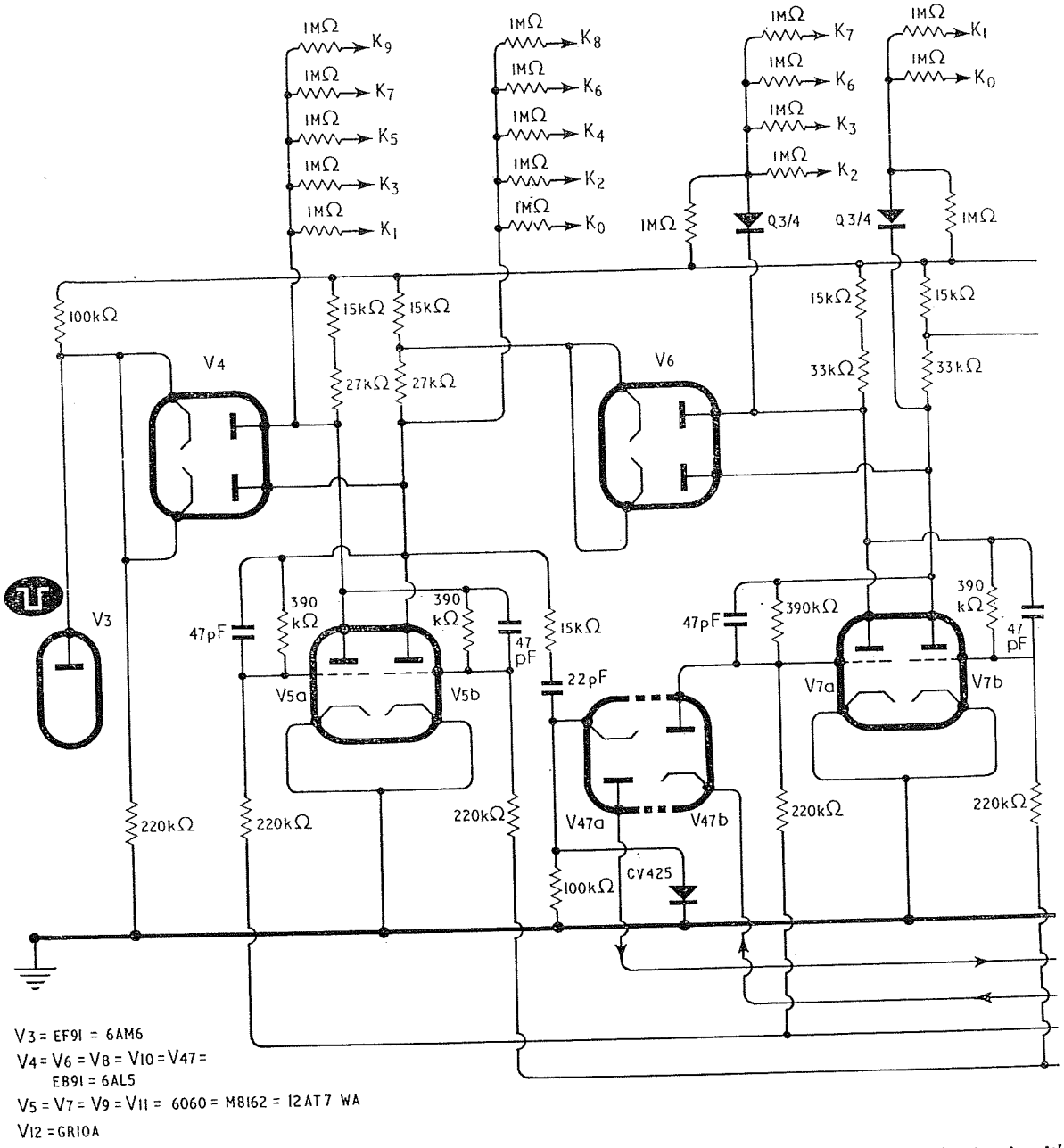
The system of readout used in the circuit of Fig. 7.5 must convert the binary electrical readout from the anodes of the binary stages into a visual decade readout. The digit to be indicated is determined by the state of a number of the binaries taken together. The circuit potentials are chosen so that



and neon readout. (Part of 1009E scaler)

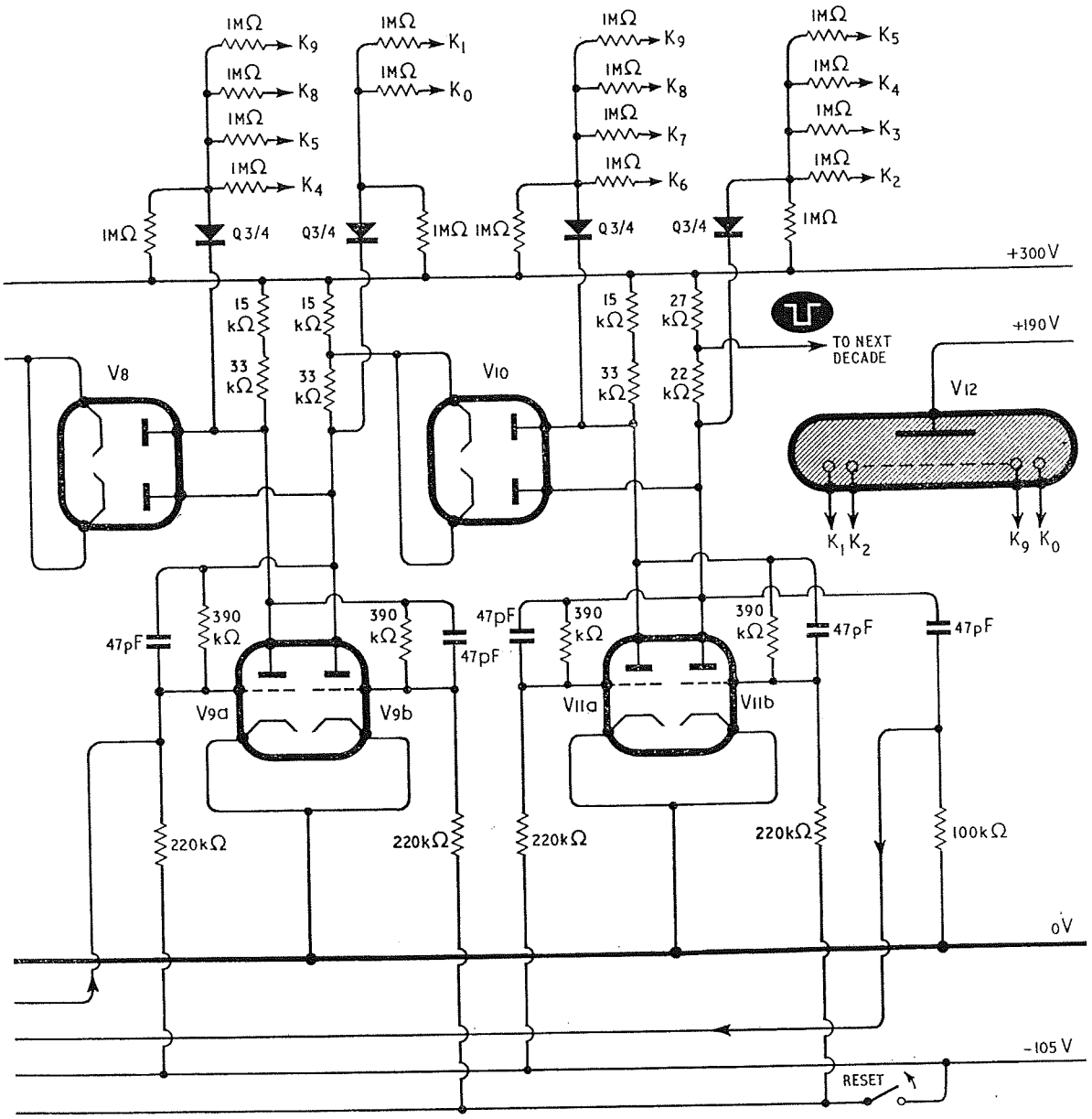
if one of the cathodes of the indicator tube is connected (via resistors) to a number of the binary tube anodes, all of these anodes must be passing current if the cathode of the indicator tube is to be at a low enough potential to glow. For example, the triodes *V*5b, *V*7b, *V*9b and *V*11b are conducting when the circuit has been reset to zero. If the zero cathode of the indicator tube is connected via resistors to the anodes of each of these triodes, the zero cathode will glow only when all four of the triodes are conducting. This occurs only when the state of the count is zero. If the connection from the zero cathode of the indicator tube to the anode of *V*5b were omitted, the cathode would glow when the other three triodes were each passing current. This occurs at counts of zero and one; the omission of the connection would, therefore, result in ambiguous indications of the state of the count. On the other hand the connection between the zero cathode of the indicator tube and the anode of *V*11b can be omitted, since the other three triodes will all conduct simultaneously only at the binary states of 0 and 8, and the 8 is one of the six binary states which have been eliminated by the feedback.

As another example, the state of the circuit can be considered after five input pulses when *V*5a, *V*7b, *V*9a and *V*11b are conducting. If all four anodes are connected to the fifth cathode of the



V3 = EF91 = 6AM6
V4 = V6 = V8 = V10 = V47 = EB91 = 6AL5
V5 = V7 = V9 = V11 = 6060 = M8162 = 12AT7 WA
V12 = GR10A

Fig. 7.5 A valve decade circuit with



GR10A readout. (Part of Ecko N530F scaler)

Table 7.1 THE TEN STATES OF THE CIRCUIT OF FIG. 7.5

No. of Input Pulses	*State of Circuit as a Binary Number*	*Possible Intermediate States*
0	0 0 0 0	
1	0 0 0 1	
2	0 0 1 0	
3	0 0 1 1	
4	0 1 0 0	
5	0 1 0 1	(0 1 0 1←)
6	1 0 1 0	
7	1 0 1 1	
8	1 1 0 0	(1 1 0 1←)
9	1 1 0 1	
10	0 0 0 0	(0 0 1 0)

indicator tube, this cathode will glow only after five pulses have been received. If the connection to $V5a$ were omitted, it would also glow after four pulses had been received and the count would be ambiguous. On the other hand, if the connection from the fifth cathode of the indicator tube to $V7b$ is omitted, the cathode will glow when the circuit is in the binary states of 5 and 7. The binary state of 7 has been eliminated by feedback, however, so the fifth cathode need only be connected to the other three anodes and a glow will be obtained from it only after five input pulses have been received.

By similar reasoning it can be shown that each cathode of the indicator tube need be connected to only three of the anodes of the tubes in the four binaries. The necessary connections are shown in Fig. 7.5. Except in the case of the first binary stage,

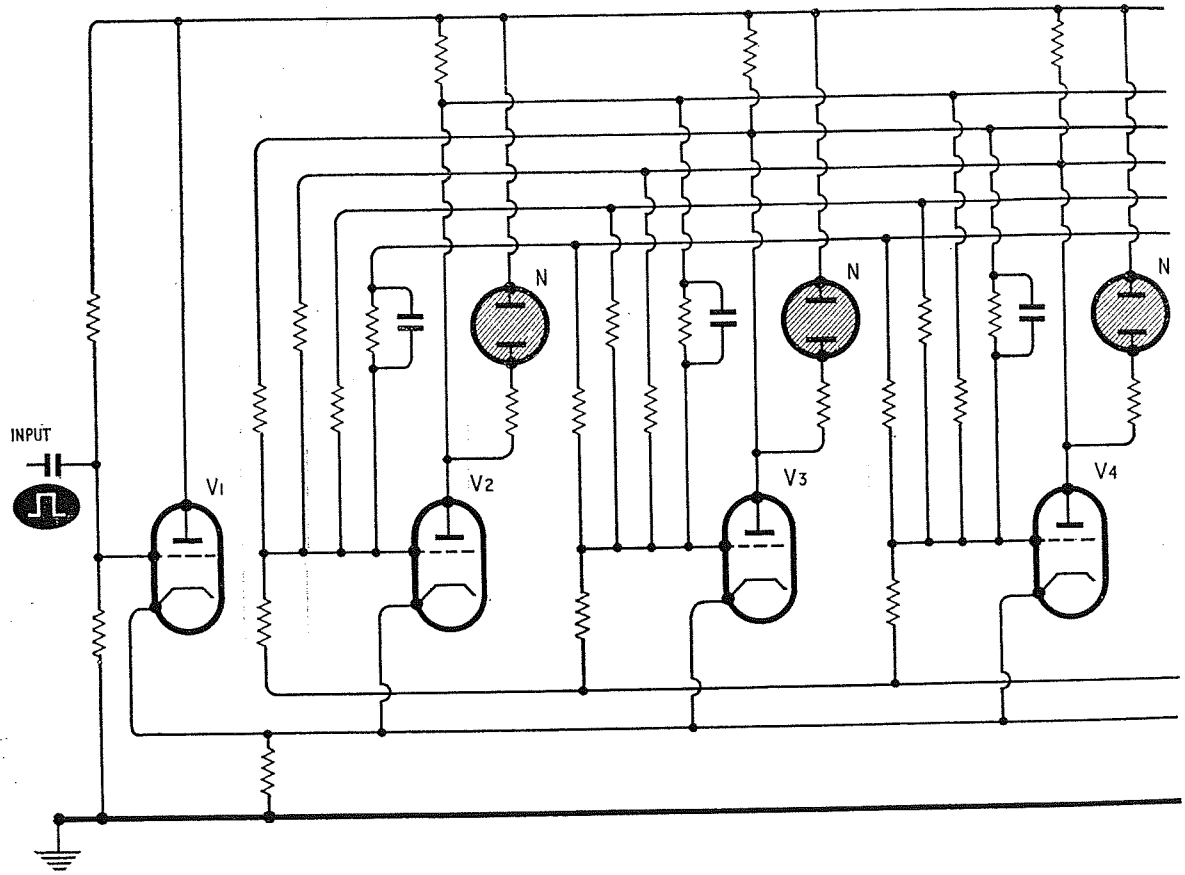
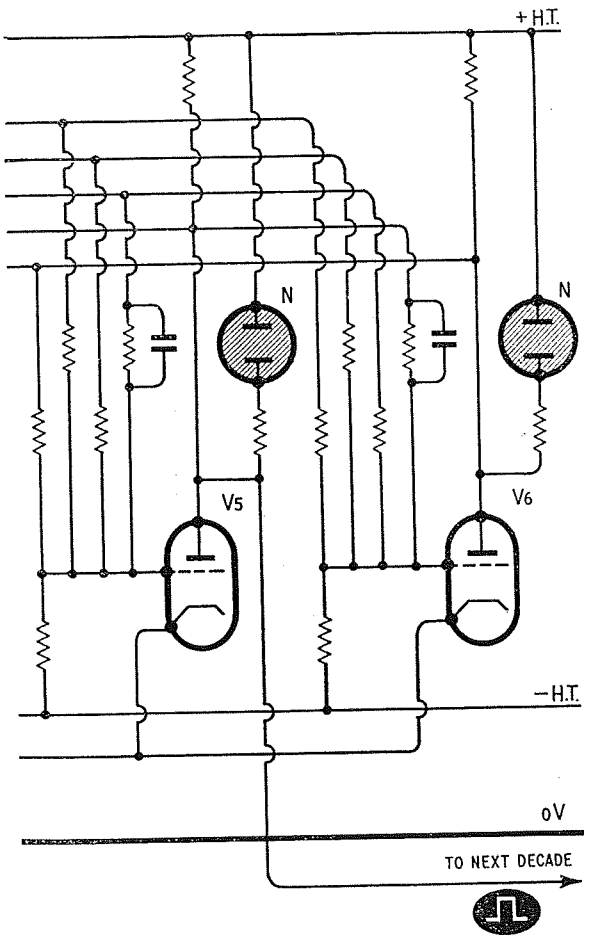


Fig. 7.6 A ring of five hard valves

the anodes of the binaries are connected to the cathodes of the indicator tube via diodes which help to remove any loading and reduce stray glows on the non-conducting cathodes.

In the N530F scaler the decade shown in Fig. 7.5 is followed by a very similar decade, also with GR10A readout, but the forward coupling is effected by means of capacitors instead of diodes, since the maximum speed at which the second decade is required to operate is one tenth of that of the first decade. In addition, longer time constants (larger resistors) are used in the second decade so that the power consumption is smaller.

7.2 VALVE RING COUNTING CIRCUITS



with neon tube readout

It is possible to construct ring circuits using hard valves, but such circuits tend to be very complicated if many stages are required in each ring. The bistable circuit is effectively a ring of two stages. The ring circuit of Fig. 7.6 functions on similar principles, but contains more tubes in the ring. Such a circuit must be arranged so that when one triode conducts all of the others receive a bias which is sufficient to prevent them from passing a current. Suitable forward coupling must also be arranged.

Although the circuit of Fig. 7.6 is not particularly simple, there are only five tubes in the ring. The neons marked *N* provide the readout. The valve *V*1 is a cathode follower which provides pulses to the cathodes of all the valves in the ring. If one valve is conducting, the fall of potential at its anode is communicated to the grids of all the other triodes in the ring by means of the potential dividing resistors; this ensures that all of the other valves are cut off. The grid of the conducting valve is connected to the anodes of the non-conducting valves which are at the potential of the H.T. line. Thus when any one valve conducts, the state of the circuit is a stable one.

Positive going pulses applied at the input pass through *V*1 and the common cathode potential of all the valves is raised. The valve which was previously conducting is thus cut off. The grid potentials of the other valves are thereby raised, but they do not conduct owing to the high common cathode potential. The resistor connecting the anode of one valve to the grid of the succeeding valve is, however, bridged by a capacitor and for a short time the full positive pulse at the anode of the valve which has been cut off is passed to the grid of the succeeding valve which conducts in spite of its high cathode potential. The anode to grid connections ensure that once a valve has commenced to conduct, it will conduct until another input pulse cuts it off.

When *V*6 is conducting the circuit is in its zero state. If *V*5 is conducting and an additional input pulse is received, the potential of the anode of *V*5 will rise as the valve is cut off; this positive going pulse can be used to operate the next ring of valves. The ring may be reset by the application of a positive going pulse to the grid of *V*6.

Ring circuits using triodes can operate at mode-

rately high frequencies (up to about 100 kc/s), but in practice the number of stages which can be incorporated in each ring is very limited. In Fig. 7.6 a resistor is employed to connect the anode of each valve to the grid of every other valve. If the number of stages is increased to twelve, 132 anode to grid resistors will be required. Apart from the resulting circuit complexity, such arrangements do not function satisfactorily owing to the excessive loading imposed on each anode circuit by the potential dividing resistors and the consequent reduction of gain in the feedback loop. A ring containing more than about seven valves is, most difficult to design.

Valve ring circuits can also be designed with one valve cut off and the remainder conducting. The current consumption and hence the heat dissipated is greatly increased, but more current is available for switching the valves. In large rings oscillations can occur in which each valve conducts in turn.

7.2.1 Ring of Bistable Circuits

Although a single high vacuum valve does not exhibit two characteristic stable states, valves may be used in pairs in multivibrator bistable circuits, each pair of valves being used as one element of the ring.

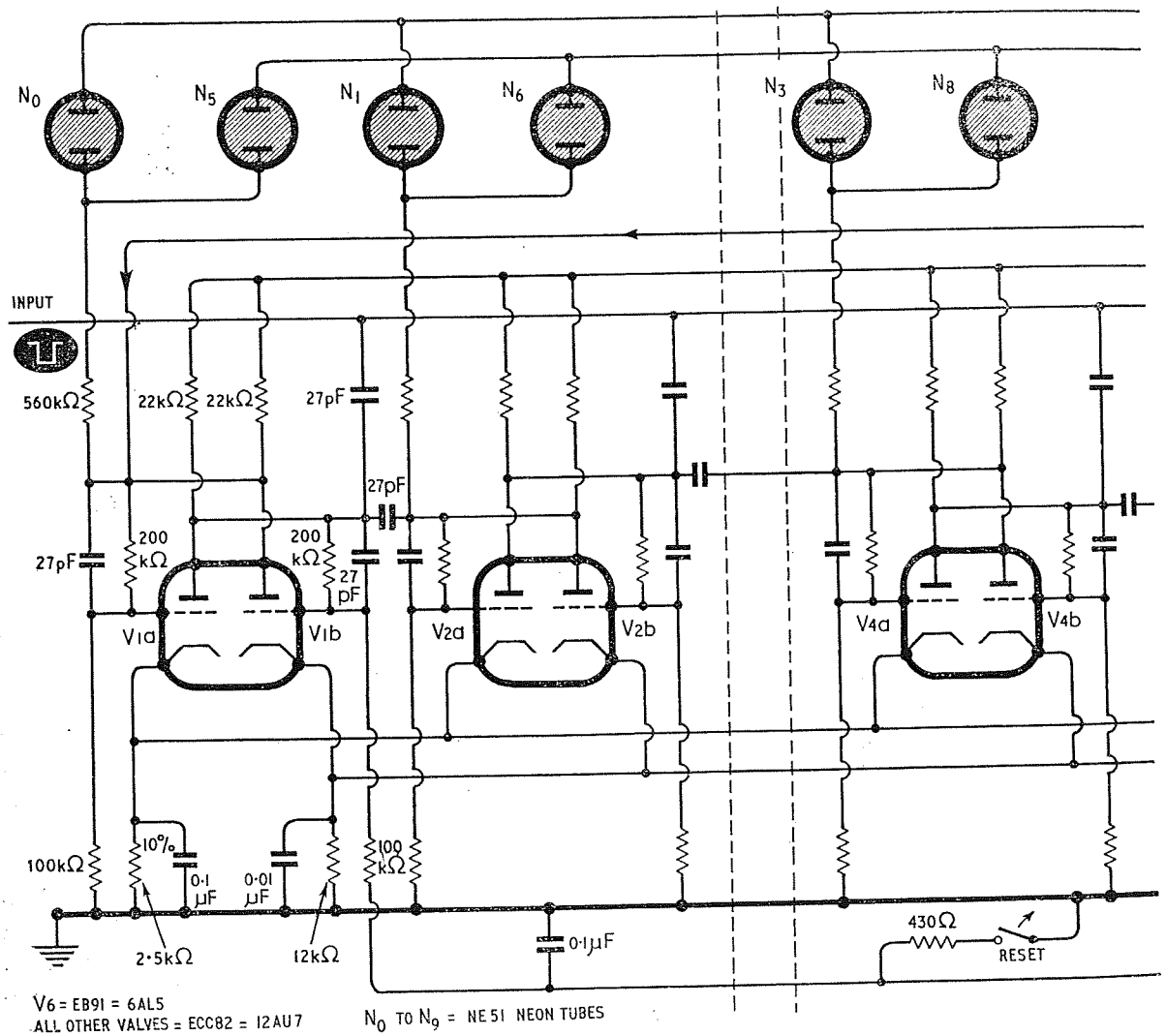
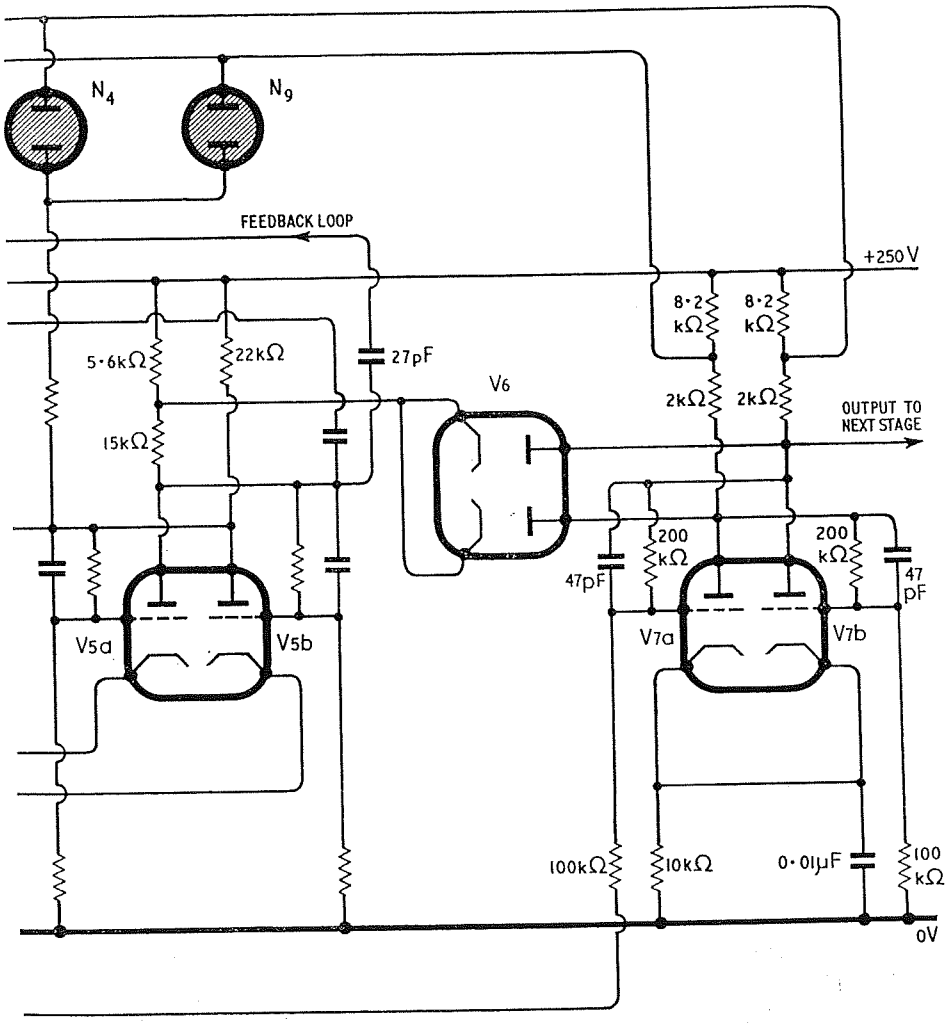


Fig. 7.7 A decade circuit comprising six multivibrators. (Values unmarked

Such a ring may contain any number of bistable circuits, but the number of valves required is twice the number of states in the ring.

The decade circuit of Fig. 7.7[6] consists of a ring of five bistable circuits (*V*1 to *V*5) followed by a single bistable circuit (*V*7). A decade can thus be constructed using a total of six multivibrators, whereas if a ring of ten is employed, ten multivibrators would be required. The maximum operating frequency of the circuit shown is about 200 kc/s. The output pulses are suitable for the direct operation of a similar succeeding decade.

The negative going input pulses are applied to the anodes of the left-hand triodes of the ring of five via the capacitors connected to the input line and are coupled to the grids of the right-hand triodes via the capacitors and resistors. At any one time one of the five right-hand triodes *V*1 to *V*5 is conducting; let us assume that it is *V*2b. An input pulse will result in *V*2b being cut off and *V*2 being switched to its quiescent state. The resulting negative going pulse at the anode of *V*2a passes through the coupling capacitor and cuts off *V*3a; *V*3 is thus switched to indicate a count. The negative going input pulses are fed to the grids of all the right-hand triodes, but have no effect on the tubes which are cut off. The input pulses are also coupled to the grids of the conducting left-hand triodes, but are atte-



are the same as those surrounding V_1)

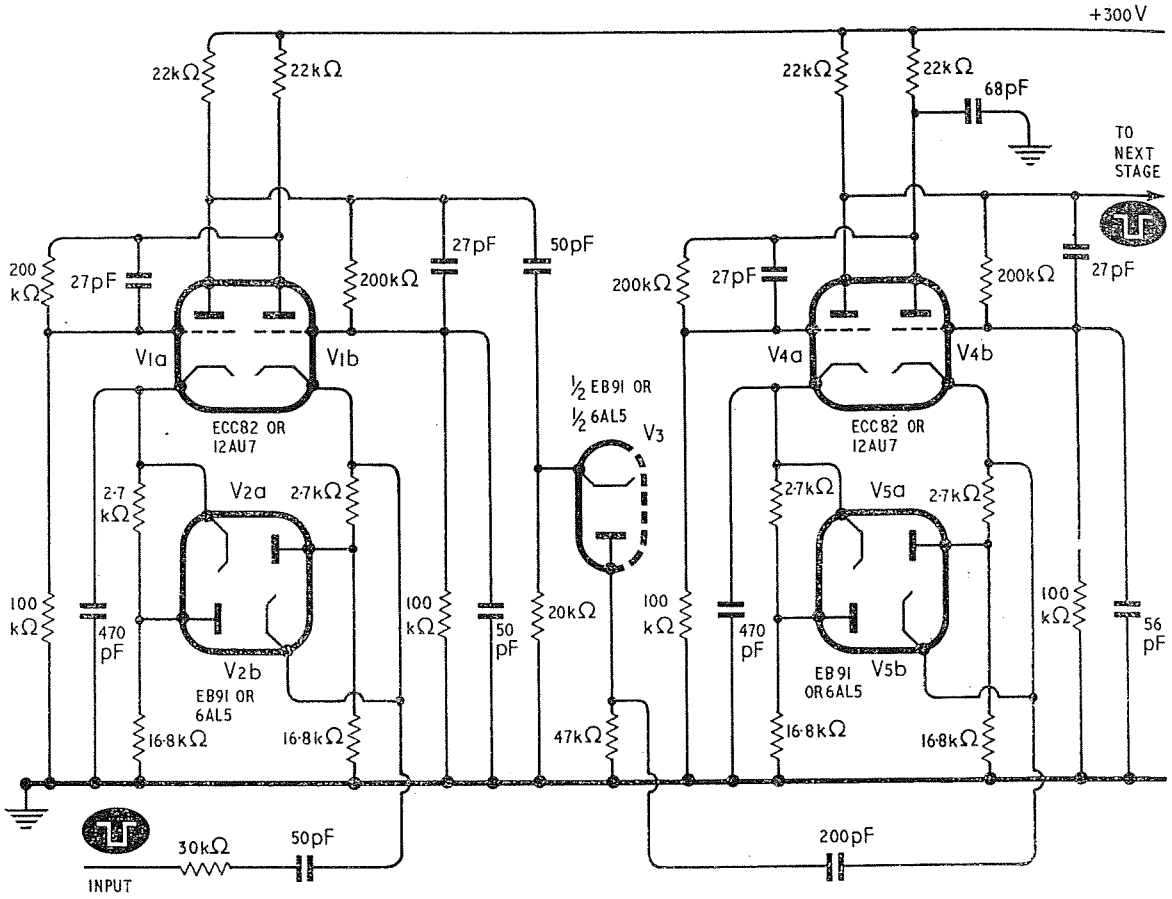


Fig. 7.8 Two cascaded ternary circuits

nuated so much by the coupling components in series with the grid resistance of the valve (which is taking grid current) that they produce no effect at all.

When $V5$a is cut off, a positive pulse occurs at its anode, but cannot pass through $V6$. If $V5$a is now switched back to its quiescent conducting state, the resulting negative going pulse passes through $V6$ to whichever anode of $V7$ is not passing a current. $V7$ thus changes its state each time $V5$ is returned to its zero state. A neon tube will glow only when the anode of $V7$ to which it is connected is cut off and when the right-hand valve of the multivibrator in the ring of five to which it is connected is conducting. During the first four pulses $V7$a conducts and successive pulses will transfer the glow from N_0 to N_4. During the next five pulses $V7$b conducts and the neons N_5 to N_9 will glow in succession. A tenth pulse resets the circuit to zero. A neon will strike when the potential difference across it is about 90 V. The anode potential of the valves in the ring varies from about 130 V (conduction) to 250 V. The voltage applied to the neons from the tapping on the anode resistor of the conducting triode of $V7$ is about 195 V.

The output taken from $V7$b will consist of one negative pulse for each ten input pulses. The reset circuit must reset both the ring of five and the bistable circuit of $V7$.

7.2.2 Valve Ternary Circuit

Ternary circuits operate on the scale of three, the only digits used being 0, 1 and 2. Circuits which operate on the scale of three can be constructed using two cascaded multivibrators with suitable feedback to reduce the scale of four to a scale of

three or by using a ring of three trigger tubes or other, bistable devices. The name 'ternary' is, however, normally used only to refer to circuits which have three stable states per sfage. Such a circuit can be constructed by modifying a valve bistable multivibrator. In addition to the normal two states in which one of the two tubes is fully conducting, a third state can be introduced in which both tubes pass a limited amount of current. Such circuits have the advantage over valve binary stages that fewer tubes are required to count over a given scale. For example, six cascaded inernary stages count in a scale of 729, whilst six binaries count in a scale of 64.

Two cascaded ternary circuits are shown in Fig. 7.8[7]. The first ternary circuit consists of $V1$ and $V2$. This circuit is in the zero state when $V1a$ is fully conducting and $V1b$ is cut off. The flow of current through the cathode resistor of $V1a$ results in the diode $V2a$ being in its non-conducting state. $V2b$ conducts, however, since the flow of current through the cathode resistor of $V1a$ renders the anode of $V2b$ positive with respect to its cathode; the lower part of the cathode resistor of $V1a$ (that is, 16.8 kΩ) is, therefore, effectively in parallel with the cathode resistor of $V1b$.

When a negative pulse is applied to the cathode of $V1b$, this valve conducts and the normal switching operation of a multivibrator commences. When both triodes are conducting, the diodes $V2$ are cut off, since the cathodes of the diodes receive the full positive voltage developed across the cathode resistors. The full values of the triode cathode resistors therefore become effective and the gain of both triode stages falls to a value at which the switching conditions of the bistable circuit are no longer satisfied (that is, the loop gain is less than unity). Both triodes, therefore, remain conducting with an anode current at a moderate value. This is the state after one input pulse.

A second input pulse increases the current in $V1b$ so that the diode $V2a$ conducts. The effective value of the cathode resistor of $V1b$ is now reduced and the stage can switch into the state inewhich $V1a$ is blocked and $V1b$ is fully conducting.

The third input pulse applied to the $V1b$ cathode causes this tube to take grid current and the grid voltage to fall. The capacitors in the grid circuit of $V1b$ charge during the pulse and keep the grid voltage strongly negative with respect to the cathode for a short time after the end of the pulse. $V1b$ is therefore cut off and the multivibrator switches to its zero state. The negative going pulse at the anode of $V1a$ passes through the diode $V3$ and triggers the next ternary stage, $V4$.

Readout from the ternary circuit may be obtained by connecting one neon in series with a 1 MΩ resistor between the anodes of the two valves in each stage. The left-hand electrode of the neon will glow in the zero state, neither electrode will glow after the first pulse and the right-hand electrode will glow after two pulses. For ease of readout it is normally preferable to use two neons per stage so that it is not necessary to observe which electrode is glowing. A neon in series with a resistor may be connected from each anode to a supply of +235 V.

The negative going input pulses to the ternary circuit should have an amplitude of between 85 and 150 V and a duration greater than 1 μsec. The three states are well defined at anode potentials of 135, 190 and 255 V. The circuit requires about 8 mA per stage at 300 V, but will operate at H.T. supply potentials from 250 to 325 V.

Other valve circuits have been designed for counting at frequencies up to 10 Mc/s[8] and for reversible counting[9].

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8

Solid State Scaling Circuits

The circuits described in this section which use binary stages are in their zero state when the right-hand transistor of each binary is conducting.

Modern solid state scaling circuits can be designed for extremely high speed operation, consume little power and are ideally suited for use as miniature printed circuits. They, therefore, possess most of the advantages which are required for use in fast computers and in many other applications; this explains the vast interest in them at the present time.

8.1 TRANSISTOR SCALERS

A single junction transistor, like a hard valve, does not have two characteristic stable states, but a bistable circuit may be constructed by using two junction transistors. Most transistor scalers consist of sets of four cascaded bistable circuits with feedback to reduce the scale of sixteen to a scale of ten. At the moment transistor ring circuits are not so common.

A single point contact transistor (the first type of transistor to be discovered) can be used in a bistable circuit, since in a common base circuit it can have a current gain which is greater than unity without phase reversal. Although this type of transistor is suitable for use in ring circuits, very few types of point contact transistor are now available, since their reliability is poor and the spread of characteristics from transistor to transistor of the same type is large. Only junction transistors will, therefore, be considered in this chapter.

Junction transistors are, on the whole, excellent devices for use as switches. An ideal switch would have an infinite resistance when open and a zero resistance when closed. When a transistor is switched off (that is, both of the junctions are reverse biased), the collector to emitter impedance will be measured in megohms and only a small 'leakage' current flows. When both junctions of the transistor are forward biased, a large current passes and the transistor is said to be saturated (that is, saturated with current). In this state the impedance from the collector to the emitter is only a few ohms and almost all of the collector supply voltage is dropped across the collector load resistor. Under these conditions the potential of the collector with respect to the emitter is about 0.1 V, but falls somewhat with increasing base current until the latter becomes so large that it develops an appreciable voltage drop across the internal emitter resistance. Bottoming occurs when the operating point is below the knee of the collector current/collector voltage characteristic and is approximately the same as saturation. An increase in the base current of a bottomed transistor will not lead to an appreciable increase in the collector current, since in the bottomed state the collector current is almost entirely determined by the collector load and the supply voltage.

The operating point of a transistor which is being employed as a switch moves over a large part of the characteristic curve and, therefore (as in the case of valve switching circuits), the simple small signal equivalent circuits cannot be used, but more comp-

licated large signal equivalent circuits lead to good approximations to the actual behaviour[1, 2]. Most transistor bistable circuits are designed, to some extent, on a trial and error basis, since a full mathematical analysis of a switching circuit (especially a non-saturating circuit) requires a considerable effort and involves certain approximations.

Transistors employed in counting circuits are normally required to have a high maximum operating speed. This implies that they must have a high cut off frequency, since the maximum switching speed is dependent on the cut off frequency. It is also desirable that they should have a low bottoming voltage if saturated circuitry is being employed, a low leakage current and a high gain over a large part of their characteristic.

The change in the collector voltage which occurs when a transistor is switched to the conducting state takes place more rapidly than when the transistor is switched to the cut off state. If a positive going pulse is applied to the base of a saturated PNP transistor, the collector current will flow for a few microseconds before the input pulse succeeds in cutting off the transistor. This occurs because more minority carriers (holes in the case of PNP transistors) are fed from the emitter into the base region during saturation than are required to enable he collector current to flow. Owing to the forward bias of the collector–base junction, the collector will become an emitter and some carriers will return from the collector to the base. The surplus minority carriers are stored in the base region (and, in some types of transistor, also in the collector region) and are used to prolong the flow of collector current for a short time after the emitter current has been cut off.

In order to obtain higher operating speeds, the storage of minority carriers may be avoided by the use of transistors in non-saturating circuits where bottoming does not occur. This does, however, complicate the circuitry, leads to greater power dissipation in the transistors and results in smaller available output currents and less well defined voltage states. In addition the use of non-saturating circuits tends to reduce reliability somewhat[3], since bottomed circuits are unaffected by short stray pulses.

A special system of charge control transistor parameters has been proposed for switching circuits[4–8] in which the transistor is considered to be switched to the conducting state by the removal of a certain amount of charge from the base region. This takes a finite time and the charge control parameters are, therefore, useful for calculating the rise and fall times in any circuit. If they are known for one circuit, they may be calculated for any other which employs the same transistors. The expression for the delay which occurs when a bottomed transistor is cut off contains two terms one of which is associated with the transistor itself and the other with the circuit in which it is being used[1, 9, 10] The transistor term can be measured directly[11].

8.1.1 Types of Bistable Circuit

The common types of bistable circuit in which only one of the two transistors is conducting in the quiescent state at any one time can be classified

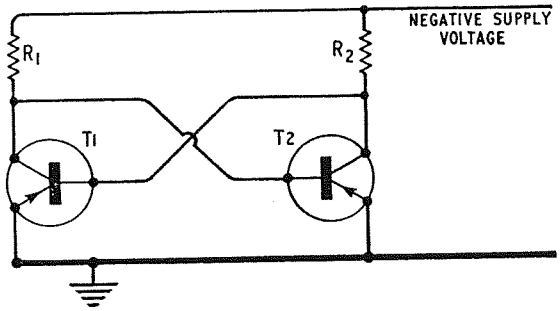


Fig. 8.1 A direct coupled multivibrator

according to the type of coupling employed, according to whether the conducting transistor is allowed to bottom or not and whether the circuit is symmetrical with respect to the two transistors. In complementary symmetry circuits both transistors conduct simultaneously. Some common types of bistable circuit will be discussed, but many variations are possible.

The simplest form of coupling between two transistors is a direct coupling from the collector of each transistor to the base of the other as shown in Fig. 8.1. This type of circuit is known as 'Direct Coupled Transistor Logic' (DCTL) and is employed only in saturated circuits.

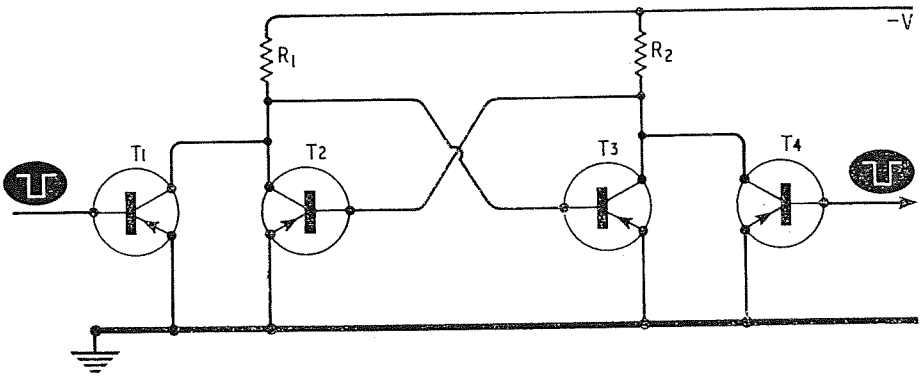


Fig. 8.2 A direct coupled binary circuit with triggering transistors

If the right-hand transistor, $T2$, is bottomed, $T1$ will pass little current. Almost the whole of the current passing through R_1 flows in the base of $T2$ which is thus kept in a highly saturated condition. In this type of circuit the collector to emitter voltage of the conducting transistor must be so small that it may be applied to the base of the other transistor without causing the latter to pass very much current.

The circuit may be switched by momentarily reducing the base current of the conducting transistor to zero so that its collector current is cut off. Two additional triggering transistors are usually used for this purpose as shown in Fig. 8.2. The additional transistors, $T1$ and $T4$, are normally in the non-conducting state. If $T2$ is conducting and $T3$ non-conducting, a negative pulse applied to the base of $T4$ will allow this transistor to conduct for a moment and take the current from R_2 which was previously passing to the base of $T2$. Thus $T2$ is cut off and a current commences to flow through R_1 and the base of $T3$. The circuit is thus switched.

A practical binary circuit using this type of coupling is shown in Fig. 8.3[12]. The capacitors C_1 and C_2 are charged to the collector potentials of the transistors. Negative input pulses applied to the base of $T5$ will cause this transistor to conduct and hence

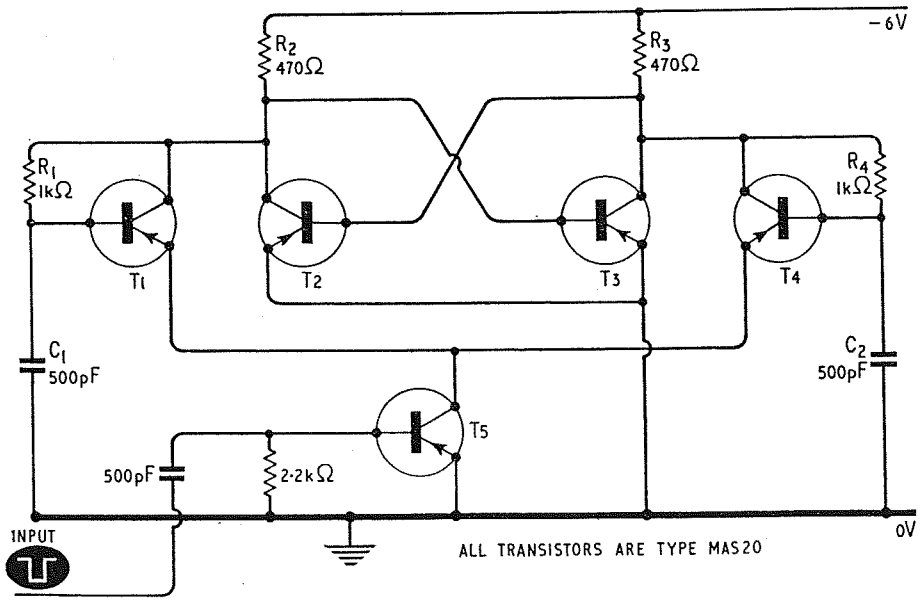


Fig. 8.3 A practical DCTL binary circuit

the emitters of $T1$ and $T4$ will effectively be earthed. If $T2$ is conducting, $T4$ will conduct during the pulse owing to its negative collector potential. The base current ceases in $T2$ with the result that the binary changes its state. The values of C_1 and C_2 must be large enough to hold the bases of $T1$ and $T4$ at a steady potential during the switching operation, but if they are too large in value, the resolving time will be increased. The circuit shown has a maximum frequency of about 2.5 Mc/s and the power dissipated in each transistor is about 5 mW.

In direct coupled circuits the conducting transistor must heavily saturate so that the base current is nearly equal to the collector current. The speed of operation is therefore limited, since a heavily saturated transistor has a relatively large stored charge in the base region. The voltage ratings of the transistors may be small, since the voltage swings

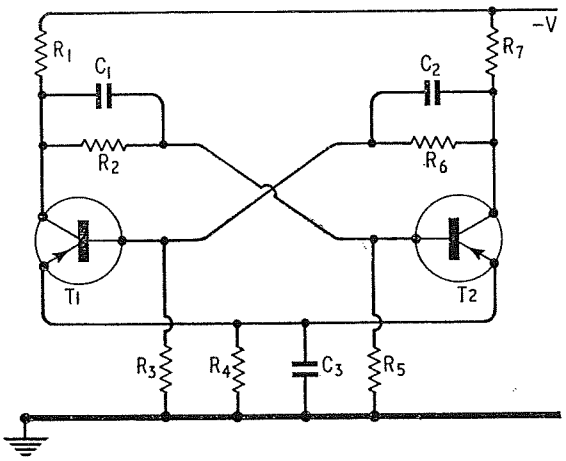


Fig. 8.4 A RCTL bistable circuit

are small. The circuit has the disadvantages that it is very susceptible to stray pulses owing to the small voltage changes and, if germanium transistors are employed, the temperature range for satisfactory operation is somewhat limited.

Greater voltage swings can be obtained if resistors are used to couple the transistors. This system is known as 'Resistor Transistor Logic'[13] (RTL). The resulting circuit is inherently rather slow in operation, since the base capacity of the transistors takes time to charge through the coupling resistors. The circuit may, however, be speeded up by the addition of a capacitor across each of the coupling resistors as shown in Fig. 8.4. This type of circuit is the fastest and most common type of saturating transistor binary stage; it is known as 'Resistor Capacitor Transistor Logic' (RCTL). The coupling capacitors, C_1 and C_2, and resistors, R_2 and R_6, should have a time constant which is about the same as the time constant of the transistor input impedance. The amount of feedback is then independent of frequency and the high frequency components of a steep waveform can pass from the collector of one transistor to the base of the other without the waveform being appreciably distorted. The capacitor may be regarded as supplying the charge necessary to cut the transistor off.

The emitters of the transistors are returned to earth via R_4. The bias voltage developed across this resistor must be great enough to ensure that one of the transistors is completely cut off. C_3 is chosen so that the potential across R_4 is kept fairly constant during switching. The potential dividers formed by R_2 and R_5 and by R_6 and R_3 can be chosen so that the base current to the conducting transistor is limited in order to avoid heavy saturation and the consequent frequency limitations.

If PNP transistors are employed, positive going input pulses are normally used to cut off the conducting transistor, since only small positive pulses are required to overcome the small negative base to emitter voltage of a conducting transistor. If negative pulses are used to switch a non-conducting PNP transistor, however, much larger input pulses are required, since the base of a cut off transistor is receiving an appreciable positive bias. The input pulses are normally applied to the bases, but they may be applied to the collectors (as in Figs. 8.9 and 8.10), in which case a pulse of larger amplitude is required.

As in valve scalers, diode gates are normally employed to guide the input pulses alternately to each transistor. Fig. 8.5 shows a practical binary with diode gates D_1 and D_2 in which the input pulses are fed to the transistor bases[12]. If $T1$ is conducting, the collector potential will be little different from the emitter or base potentials. There is therefore little potential difference across the diode D_1 and any positive going input pulse will render D_1 conducting so that the pulse can pass to $T1$ to switch the stage.

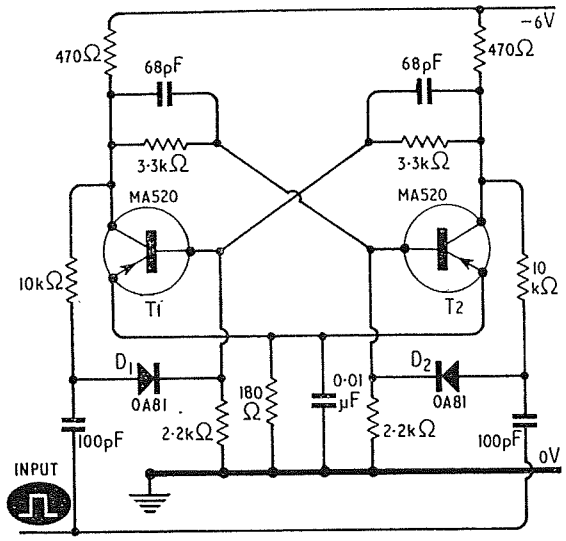


Fig. 8.5 A practical RCTL bistable circuit

The negative potential of the collector of $T2$ during the time this transistor is cut off ensures that D_2 is reversed biased; the positive input pulse cannot, therefore, pass through D_2 unless it has an amplitude which is great enough to overcome the reverse bias of the diode. The input pulses should not, therefore, be too large. When the stage has switched the transistors will interchange roles and D_1 will now be reverse biased so that the succeeding input pulse is gated to $T2$ only. This circuit will operate reliably at 4 Mc/s and will function with a supply voltage as low as 3 V.

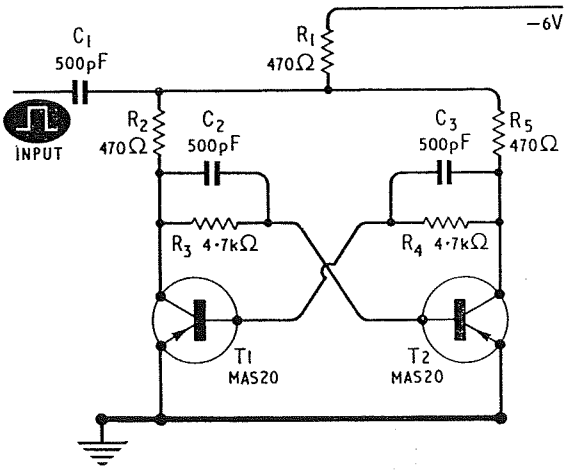


Fig. 8.6 An economical binary circuit

If the maximum operating speed is reduced, it is possible to omit the gating diodes when suitable transistors are used. An economy circuit of this type is shown in Fig. 8.6[12]. The base of each transistor is not returned to earth through a resistor and therefore the collector to emitter voltage of a saturated transistor must be so low that it does not cause the other transistor to pass appreciable current. If $T1$ is conducting, the positive going input pulse will pass through R_5 and R_4–C_3 to the base of T_1 which is thus cut off. The pulse does not appreciably affect the collector potential of the conducting transistor, $T1$, and therefore does not reach the base of the non-conducting transistor, $T2$. The input is shunted by

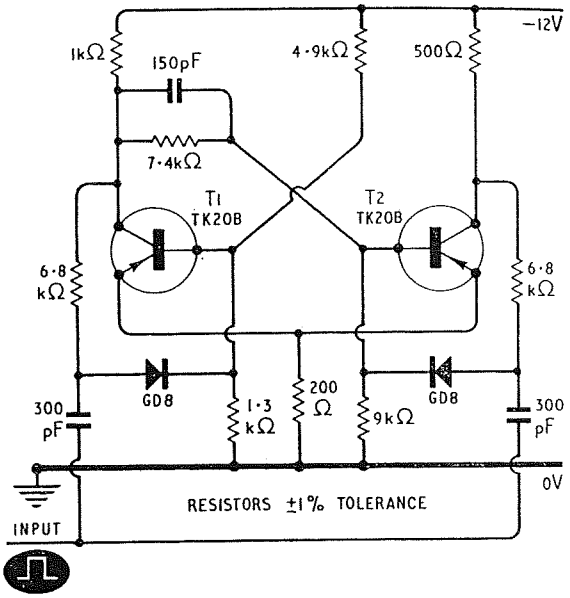


Fig. 8.7 An asymmetrical binary circuit

the resistor R_1 and by the collector load of the conducting transistor, so that sensitivity is rather low. The circuit will function at frequencies up to 1 Mc/s and requires an input pulse amplitude of about 1 V.

Asymmetrical Bistable Circuit

The common emitter resistor of Fig. 8.4 can be used to provide the feedback from one transistor to the other if the by-passing capacitor C_3 is removed. A saturating bistable circuit of this type is shown in Fig. 8.7[14]. $T2$ is a common collector amplifier and $T1$ a common base amplifier; the output from $T1$ is

coupled to $T2$. Owing to the asymmetry of the circuit, the outputs from the transistors differ in amplitude. The power consumed varies from 144 mW when $T1$ conducts to 240 mW when $T2$ conducts.

If a bistable circuit is to be operated with heavy loading on its output, it may be advantageous to employ two emitter followers to couple the output of each transistor to the input of the other [14].

Complementary Symmetry Circuits

Complementary symmetry circuits[15] employ one PNP and one NPN transistor. At any time either both transistors are conducting or both are cut off. The basic type of bistable circuit is which they are used in shown in Fig. 8.8. The whole of the collector current of each transistor is fed to the base of the

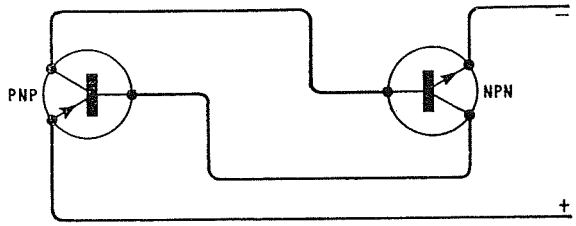


Fig. 8.8 The basic complementary symmetry bistable circuit

other. Fewer components are used than in the common types of bistable circuit and little power will be consumed if the circuit is in its non-conducting state for the majority of its operating time. The two transistors together behave as a transistor with a common base circuit gain greater than unity and can be used to replace a single point contact transistor in ring circuits, etc., such as that of Fig. 8.18. Saturated comsplemenary symmetry circuits have been designed for ue at frequencies of up to 20 Mc/s[16]. A single PNPN device is effectively the same as the two transistors of Fig. 8.8 and can be used in the same type of bistable circuits (Section 8.2).

Non-saturating Circuits

In order to obtain faster switching or greater sensitivity to input pulses, a bistable circuit may be arranged so that the transistors do not operate in the saturated condition. There are a number of ways in which saturation may be prevented, but in all of

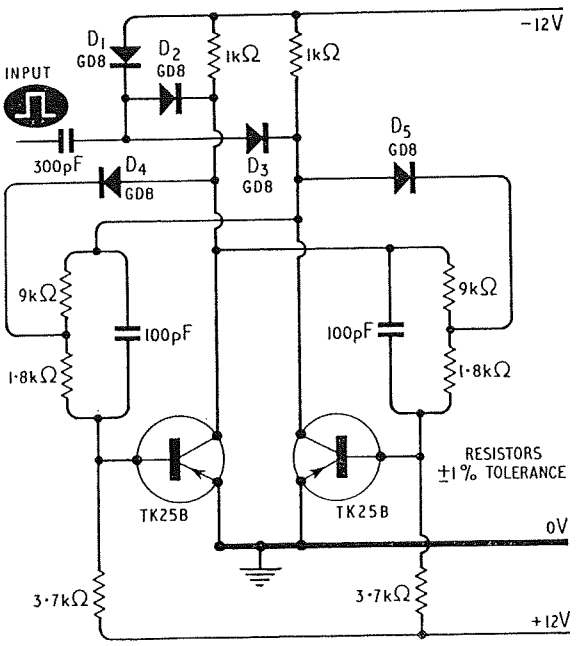


Fig. 8.9 The use of feedback to avoid saturation

them care must be taken to ensure that the power dissipated in the conducting transistor does not become excessive.

It has already been stated that saturation may be prevented in the circuit of Fig.8.4 by a suitable choice of resistor values which reduce the base current taken by the conducting transistor. Such circuits are not very tolerant of variations in transistor current gain and in order to achieve d.c. stability with transistors of low current gain, it is often necessary to accept some saturation with transistors of the same type but which have a high current gain [14]. Close tolerance resistors are desirable for this type of circuit.

In another type of circuit for avoiding saturation, the fall in potential at a collector as it approaches saturation is fed back to the base so that the collector current is decreased. A typical circuit is shown in Fig. 8.9[14]. The feedback occurs through either D_4 or D_5 and the circuit is arranged so that these diodes do not conduct until the potential of the collector falls below the potential of the tapping on the coupling resistor. Thus the feedback only takes place as saturation is approached. In this circuit the input pulses are fed to the collector of the conducting transistor via the gating diodes D_2 and D_3. D_1 clamps

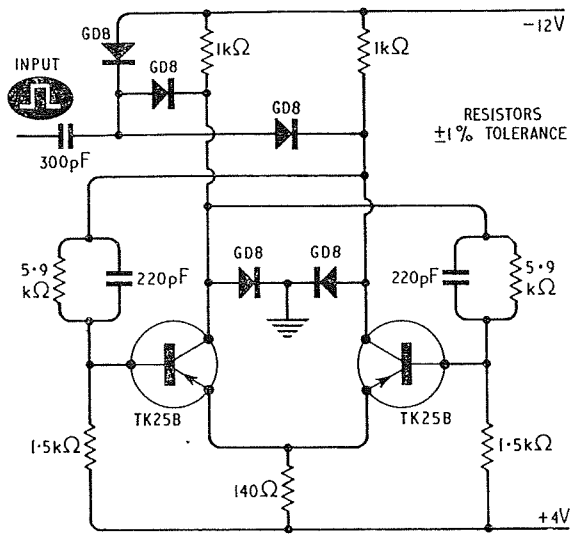


Fig. 8.10 The use of clamping diodes to avoid saturation

the left-hand sides of D_2 and D_3 to the negative supply voltage. This type of circuit has the advantage that the power dissipated at the collectors is small, since the collector current does not rise above the value which is required for bottoming. One of the disadvantages of the circuit is that the output impedance is relatively large. The maximum frequency of operation of the particular circuit shown is about 500 kc/s.

A third method for avoiding saturation involves the clamping of the collector potential by means of a diode so that it can never reach the bottoming value. The diode used should have a low minority carrier storage and a low forward resistance; a bonded diode maybe suitable. In this type of circuit a large current may pass through the diode and transistor, but this can be avoided by the use of a second diode and a resistor in the emitter circuit. In the circuit of Fig. 8.10, the base-emitter junction of the non-conducting transistor is used as the second diode[14]. The circuit is relatively independent of the transistor characteristics. In the particular circuit shown, the power dissipation is about 250 mW and the maximum operating frequency about 600 kc/s.

8.1.2 Decade Circuits

Transistor decade circuits may be constructed by applying feedback to four cascaded binary circuits according to the principles discussed in Chapter 1. The feedback system used will depend on the type of readout being employed and possibly on the operating frequency required. The maximum operating frequency of conventional decade circuits is usually a little above half the maximum operating frequency of the binaries used.

The economical decade circuit of Fig. 8.11(a)[12] may be constructed from binary circuits of the type shown in Fig. 8.6. The circuit operates as a cascaded binary counter for the first nine pulses, the pos-

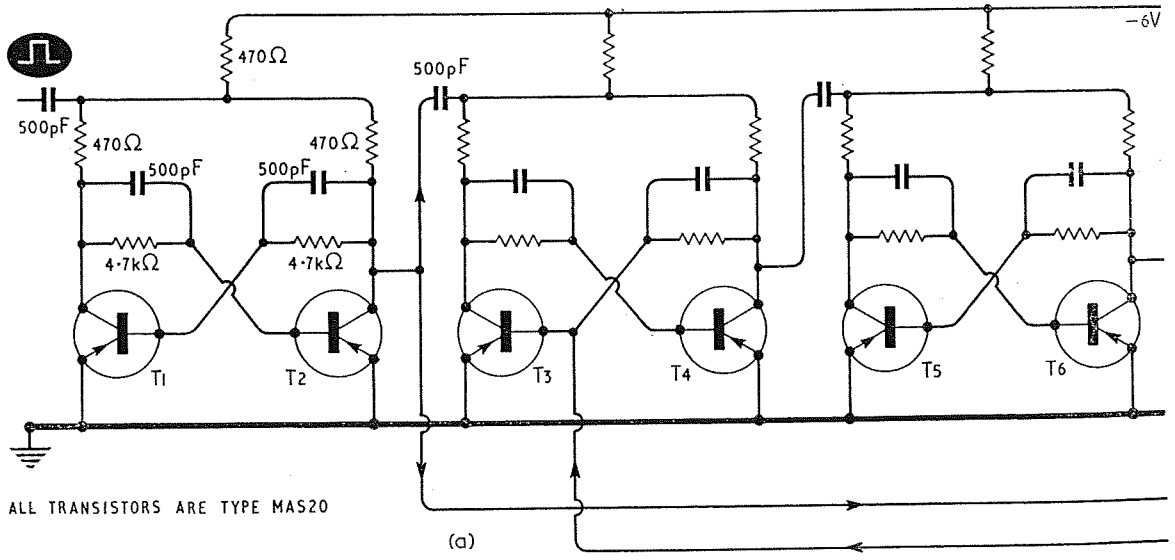


Fig. 8.11(a) An economical decade circuit. (b) An amplifier

itive output pulses from a binary passing through the coupling capacitor to the succeeding binary. $T7$ is cut off during the first seven pulses and is not affected by positive going pulses from $T2$. The fourth binary is switched by the eighth input pulse, whilst the ninth pulse merely switches the first binary. The tenth pulse returns the first binary to zero and a positive pulse from $T2$ passes through D_1 to switch the fourth binary back to zero. A positive output pulse from $T8$ is fed back to $T3$ to prevent the switching of the second binary by the pulse from $T2$. Thus the whole decade is returned to zero.

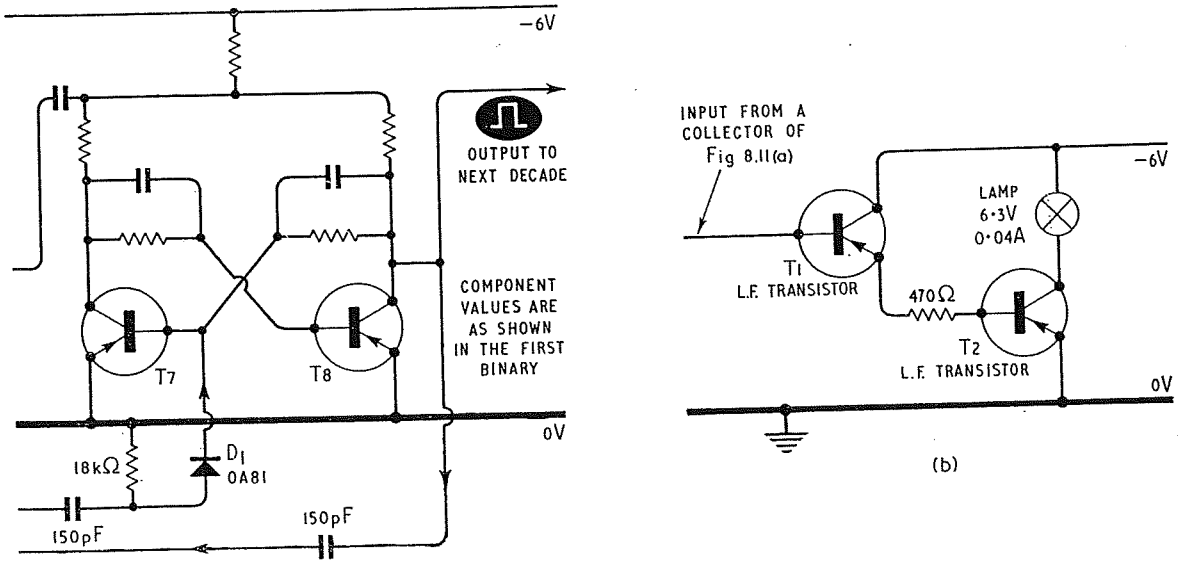
This circuit uses very few components and operates at frequencies of up to about 800 kc/s. The input pulses should have an amplitude of not less than 0.8 V.

One possible method of readout from the circuit of Fig. 8.11(a) involves the use of small tungsten filament lamps[12]. Four circuits of the type shown in Fig. 8.11(b) may be used to provide the readout without imposing an appreciable load on the binaries in the decade. One of the readout circuits is connected to the collector of the right-hand transistor of each binary in the decade. When a binary is switched from zero to indicate a count, the potential of the collector of the right-hand transistor becomes more negative (almost as negative as the power supply line) and this negative pulse can be used to switch on $T1$ of the readout circuit. The current passed by $T1$ switches on $T2$ and the bulb is thus illuminated.

This method of readout is, of course, binary in nature, the four bulbs indicating counts of 1, 2, 4 and 8. When more than one bulb is illuminated, the count is the sum of the numbers indicated by the illuminated bulbs. A similar readout system could be constructed using small neon bulbs, but high voltage silicon transistors would also be needed. Another system of readout can be constructed in which a diode matrix is employed to convert the binary readout to decimal information[12]. The outputs from the matrix may be amplified and used to operate a group of ten filament lamps which provide decade readout.

8.1.3 Meter Readout

The binary circuit of Fig. 8.5 may be used to construct decade counters of the type shown in Fig. 8.12[12]. The absence of heavy saturation enables speeds of about 4 Mc/s to be attained. This circuit employs a different feedback system to that of Fig. 8.11, since it counts only the first seven pulses in a binary manner. The eighth pulse causes the fourth binary ($T8$ and $T9$) to be switched; a negative going pulse from $T9$ is applied to $T10$ and $T5$ and the resulting current pulses are used to switch the second and third binary stages to indicate a count. The



to enable the decade to be used to control indicator lamps

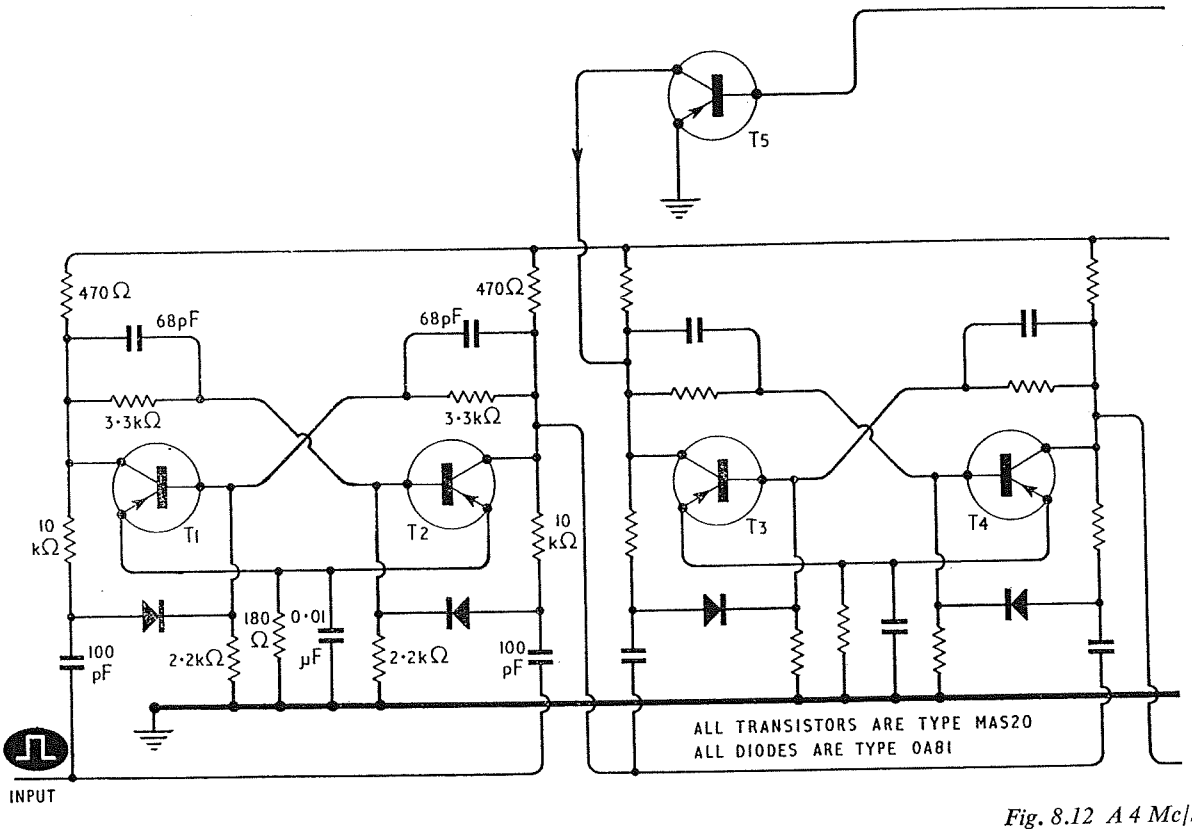


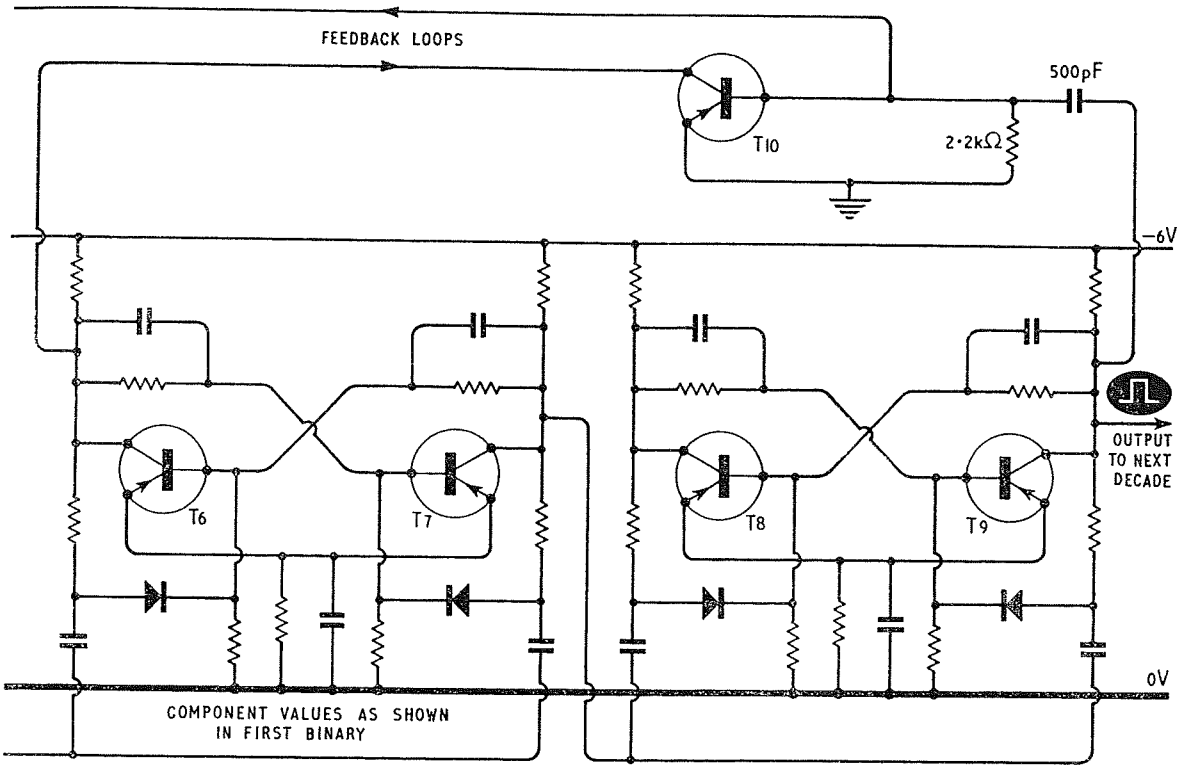
Fig. 8.12 A 4 Mc/s

decade will be switched to zero after another two pulses. The sequence of counting is in Table 8.1. It can be seen that a change of state of the fourth binary should be regarded as being equivalent to two input pulses instead of the more usual eight. The binary numbers 8 to 13 inclusive have been eliminated to convert the scale of 16 to a scale of ten.

This type of feedback system is very suitable for use with the circuit of Fig. 8.13(a) to provide meter readout. Each of the resistors in Fig. 8.13(a) is connected to the collector of the right-hand transistor of one of the binaries. When a binary is in its zero state, the right-hand transistor is bottomed and its collector is at about earth potential. Therefore, little current will pass through the meter to the binary. When a binary is not in the zero state, however, a current will flow through the meter to the collector of the right-hand transistor. This current is almost entirely determined by the resistor shown in Fig. 8.13(a) which is connected to the binary concerned. The current which passes through the resistor $R/4$ to the third binary is four times the current which passes through the resistor R to the first binary and twice the current which passes through one of the resistors $R/2$ to either the second or fourth binaries when the binaries concerned are not in their zero state. The total current passing through the meter is, therefore, proportional to the number of pulses which have been applied at the input.

Table 8.1

State of binaries	*Count*
0 0 0 0	0+0+0+0 = 0
0 0 0 1	0+0+0+1 = 1
0 0 1 0	0+0+2+0 = 2
0 0 1 1	0+0+2+1 = 3
0 1 0 0	0+4+0+0 = 4
0 1 0 1	0+4+0+1 = 5
0 1 1 0	0+4+2+0 = 6
0 1 1 1	0+4+2+1 = 7
1 1 1 0	2+4+2+0 = 8
1 1 1 1	2+4+2+1 = 9
0 0 0 0	0+0+0+0 = 0



decade circuit

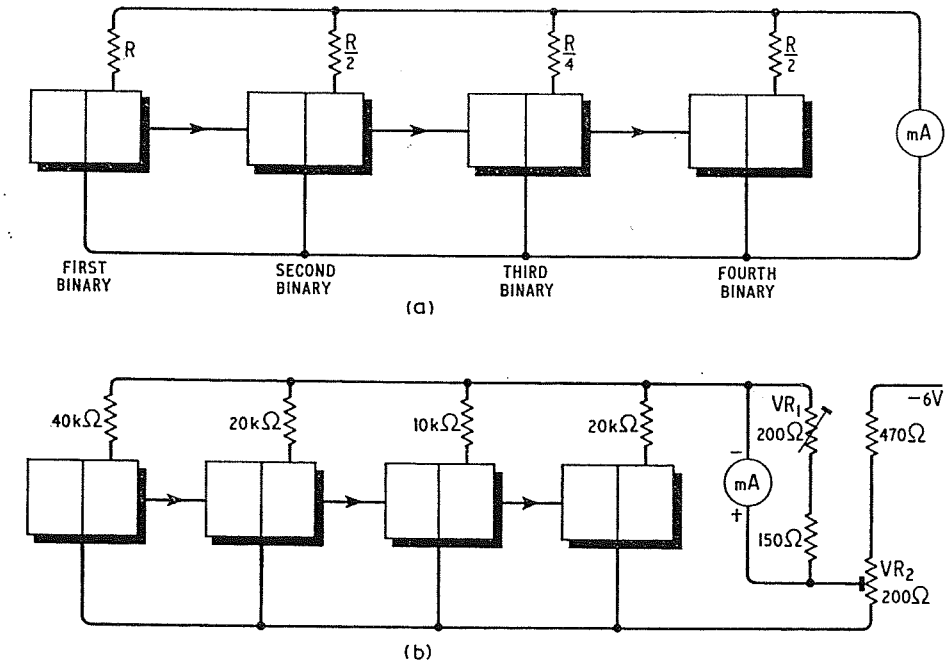


Fig. 8.13(a) The basic circuit for meter readout. (b) Practical circuit for meter readout from Fig. 8.12

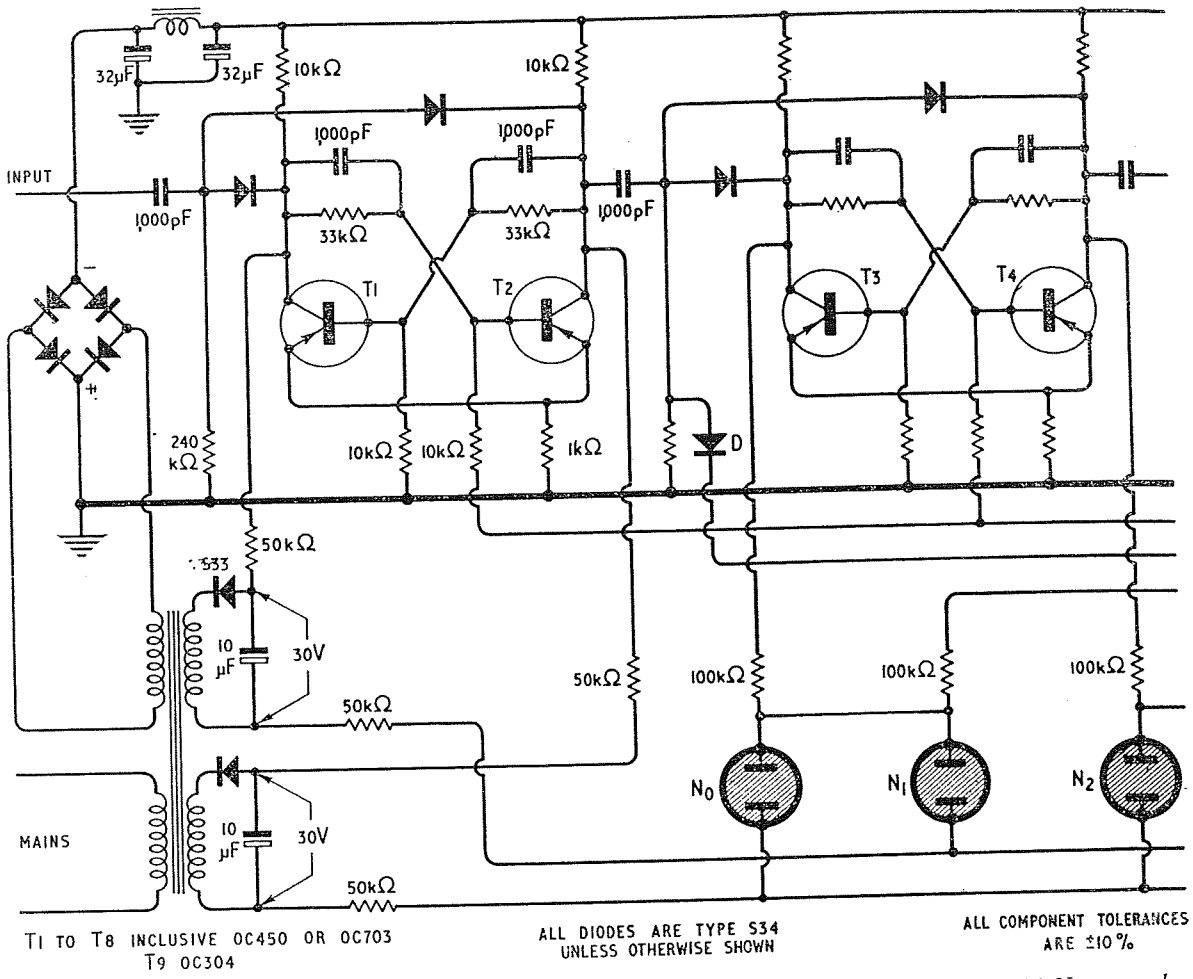


Fig. 8.14 Neon readout

In actual practice the meter should be returned to a potentiometer, VR_2, as shown in Fig. 8.13(b), since the potential of the collector of a conducting transistor is not quite zero. The potentiometer VR_1 is provided so that the current can be adjusted to give a full scale deflection of the meter when all of the right hand transistors are conducting. The meter should have a full scale deflection of 0.5 mA and a resistance of 175 Ω. Ideally it should be scaled from 0 to 9. A stable power supply voltage is required, since the meter deflection depends on the voltage.

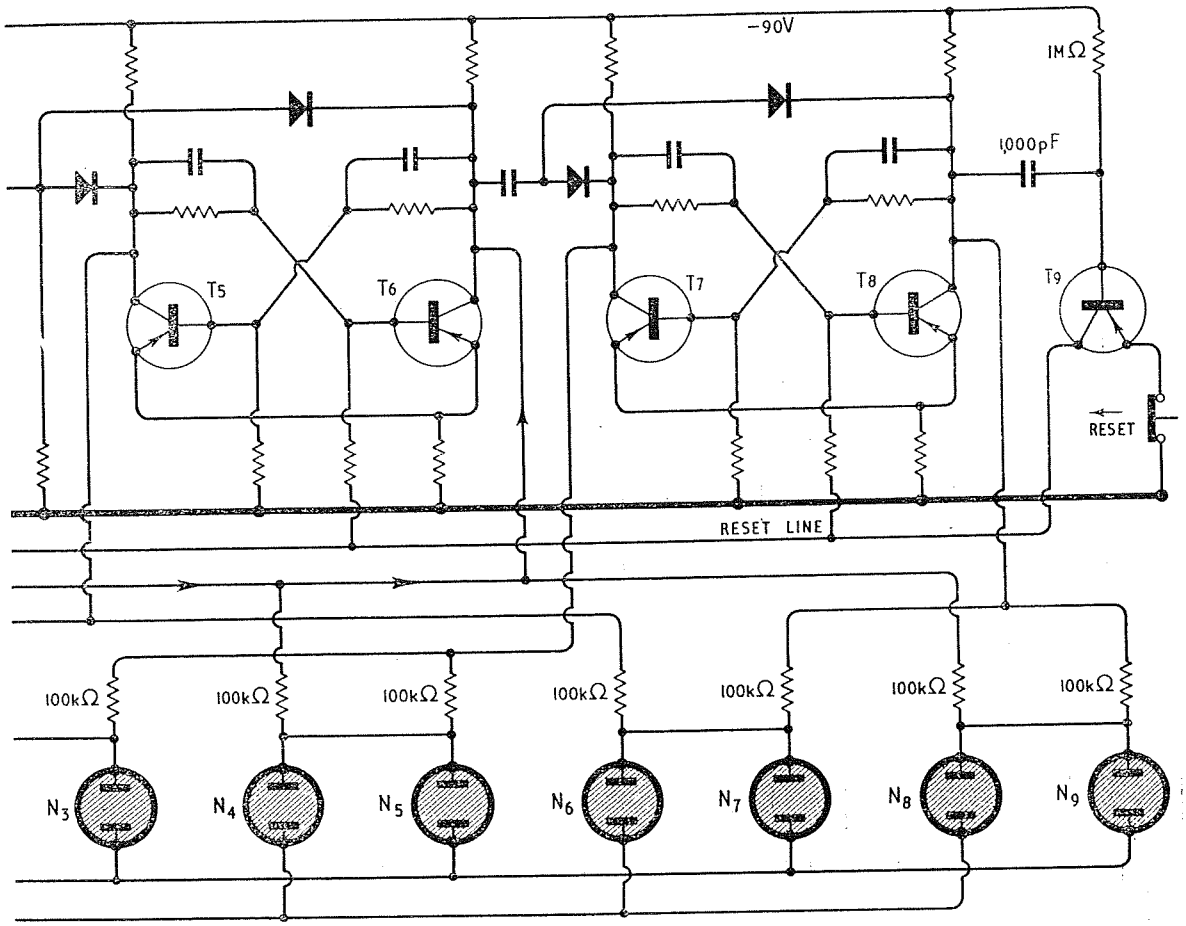
Meter readout can be used in the circuit of Fig. 8.11(a), but the resistor connected between the meter and the fourth binary must be one eighth of the value of that connected to the first binary.

DCTL Decade

Four binaries of the type shown in Fig. 8.3 may be combined to form a decade counter using the same feedback system as that of Fig. 8.12[12]. The circuit is exactly similar to that of Fig. 8.12, but the output pulses from each binary are taken from the left-hand transistors, since negative pulses are required. They are coupled into the succeeding stage by 500 pF capacitors. The maximum operating speed is about 1.5 Mc/s.

8.1.4 Neon Readout

Many transistor scalers operate with collector voltage swings of a few volts and cannot, therefore, operate small neon tubes, since the minimum volt-



from a transistor decade

age required to ignite such tubes is of the order of 70 V. Such potentials can, however, be generated by decade circuits employing silicon transistors[17]. Four neon tubes may be used to provide binary readout or ten tubes may be used to provide decade readout.

A circuit which employs OC405 or OC703 transistors to provide decade readout using ten neons is shown in Fig. 8.14[18]. It has a maximum speed of about 35 kc/s. The base of the reset transistor, *T*9, normally receives a bias current from the negative supply line via the 1 MΩ resistor. The transistor, therefore, conducts and effectively connects the reset line to earth. If the reset switch is opened, the bases of the right-hand transistors become negative and the circuit is reset to zero.

The circuit of Fig. 8.14 counts only the first five pulses in a binary manner. At the sixth input pulse the output from the first binary switches the second and third binaries. Positive pulses can pass from the first binary through the diode *D* to the third binary only when latter is not in its zero state. The next three pulses are counted in a binary manner, but at the tenth pulse the same feedback process occurs from the first to the third binary which leaves the circuit in the binary state 0010. When the fourth binary switches to zero, however, *T*8 provides a positive pulse which stops the flow of current from the negative supply line to the base of *T*9. This transistor becomes non-conducting and the second binary is reset to zero. The counting sequence is shown in Table 8.2

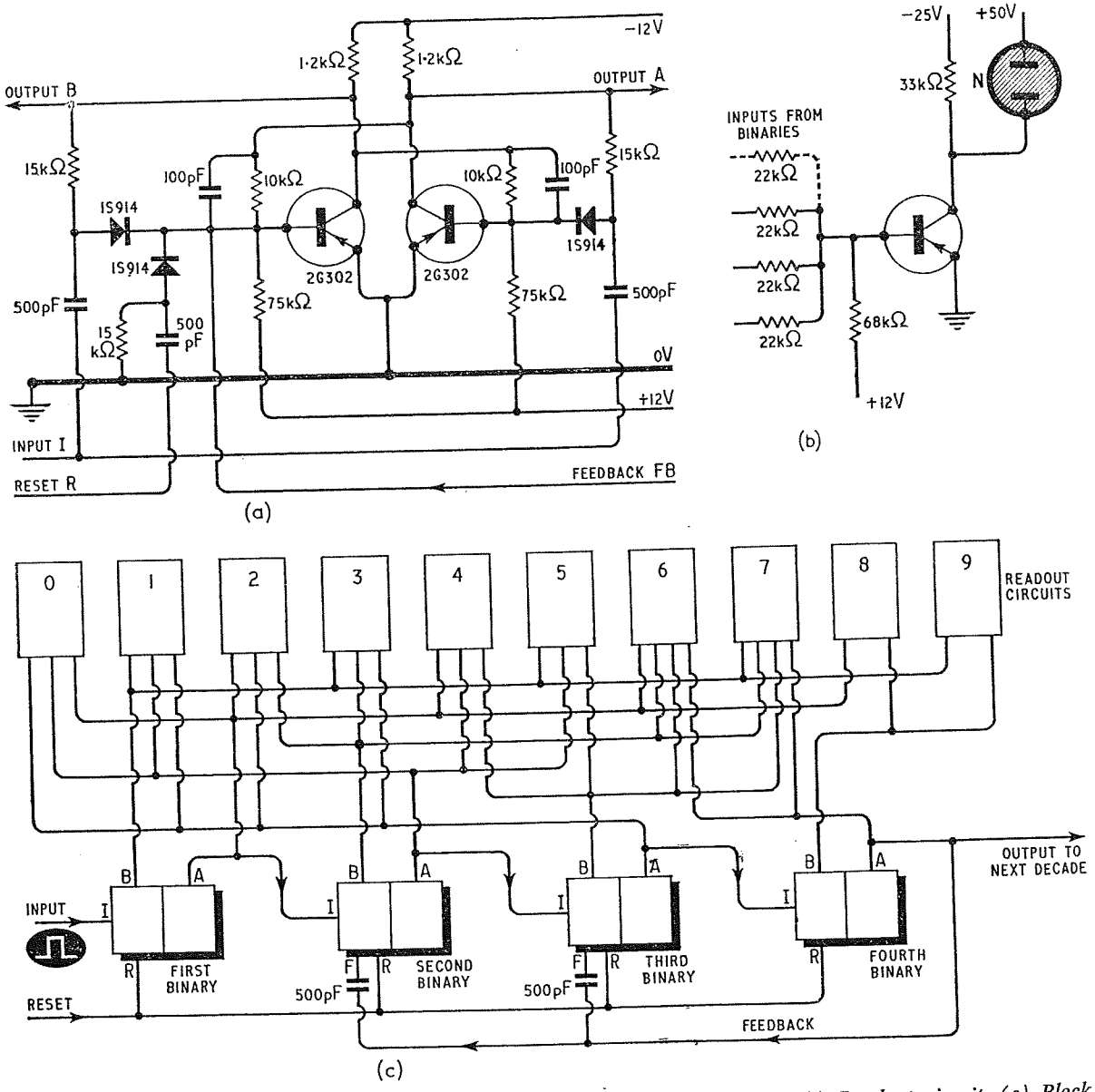


Fig. 8.15 A 200 kc/s decade with neon readout. (a) Circuit of saturating binary, (b) Readout circuit, (c) Block diagram of complete counter

Table 8.2

No. of pulses	*State of the binaries*
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	1 0 1 0
7	1 0 1 1
8	1 1 0 0
9	1 1 0 1
10	(0 0 1 0)
	0 0 0 0

The six binary numbers omitted from the scale of sixteen are therefore 6, 7, 8, 9, 14 and 15.

This decade operates from a −90 V supply. The potential of the emitters of the binaries is about −10 V with respect to earth and the potential of the conducting collectors is little different from this. The potential of a cut off collector is about −70 V.

Neon tube decade readout may be obtained from this circuit as shown in Fig. 8.14. The anodes of the even numbered neons are all connected to a floating source of a constant potential of about 30 V. The other side of this source is connected to the right-hand transistor of the first binary. The anodes of the odd numbered neons are connected to a similar source of potential which is returned to the left-hand transistor of the first binary. In the zero state the potential of the anodes of the even numbered neons is therefore (−10+30) = +20 V with respect to earth. The cathodes of the odd numbered neons are at (−70+30) = −40 V with respect to earth. Each time the first binary switches these voltages will be interchanged. The cathodes of the neons are connected via resistor networks to the collectors of transistors in the second, third and fourth binaries.

The voltages developed across each neon for each state of the decade is shown in Table 8.3. If the neons have an ignition voltage of between 70 and 80 V, it can be seen that the appropriate neon and no other will ignite to indicate the state of the count. The current passing through a neon (about 100 μA) is determined by the two 100 kΩ resistors connected to the cathodes of each neon and the 50 kΩ resistors in the neon anode leads. The two windings for the 30 V supplies should be screened from the other transformer windings.

Another type of circuit employing decade neon readout is shown in Fig. 8.15[19]. The transistors used in the binaries operate from low voltage supplies and a transistor amplifier is, therefore, required to operate each neon. Four of the binaries and ten of the readout circuits are connected as shown in the block diagram of Fig. 8.15(c). The first seven pulses are counted in a binary manner, but the eighth pulse switches the fourth binary and a signal is fed back to switch both the second and third binaries. The operational sequence is the same as that used in the circuit of Fig. 8.12. The neon tubes used should ignite when the applied voltage is between 50 and 75 V. The maximum counting frequency is about 200 kc/s.

Table 8.3

State of Decade	N_0	N_1	N_2	N_3	N_4	N_5	N_6	N_7	N_8	N_9
0	**90**	30	60	0	60	0	60	0	60	0
1	30	**90**	0	60	0	60	0	60	0	60
2	60	0	**90**	30	60	0	60	0	30	−30
3	0	60	30	**90**	0	60	0	60	−30	30
4	60	0	60	0	**90**	30	30	−30	60	0
5	0	60	0	60	30	**90**	−30	30	0	60
6	60	0	60	0	30	−30	**90**	30	60	0
7	0	60	0	60	−30	30	30	**90**	0	60
8	30	−30	30	−30	60	0	60	0	**90**	30
9	−30	30	−30	30	0	60	0	60	30	**90**

8.1.5 Numerical Indicator Tube Readout

Many types of numerical indicator tube can be driven from a low voltage transistor scaler if a diode matrix is employed to convert the binary readout to decimal readout. Ten NPN transistors are also required to amplify the currents from the matrix so that they are large enough to operate the indicator tube. A typical circuit[20] for operating the GR10H tube is shown in Fig. 8.16. The scaler should count in the binary manner up to nine and be reset at the tenth pulse. The circuit is designed to operate with a collector voltage swing of the binary transistors between −1.5 V and the earth potential. A few indicator tubes (such as the GR10G) are not very suitable for use in this type of circuit, since there is a large amount of ionisation coupling between adjacent cathodes and a large bias is required on the unused cathodes.

The use of the Z550M which has been specially developed for providing readout from transistor scalers will be discussed in Chapter 10.

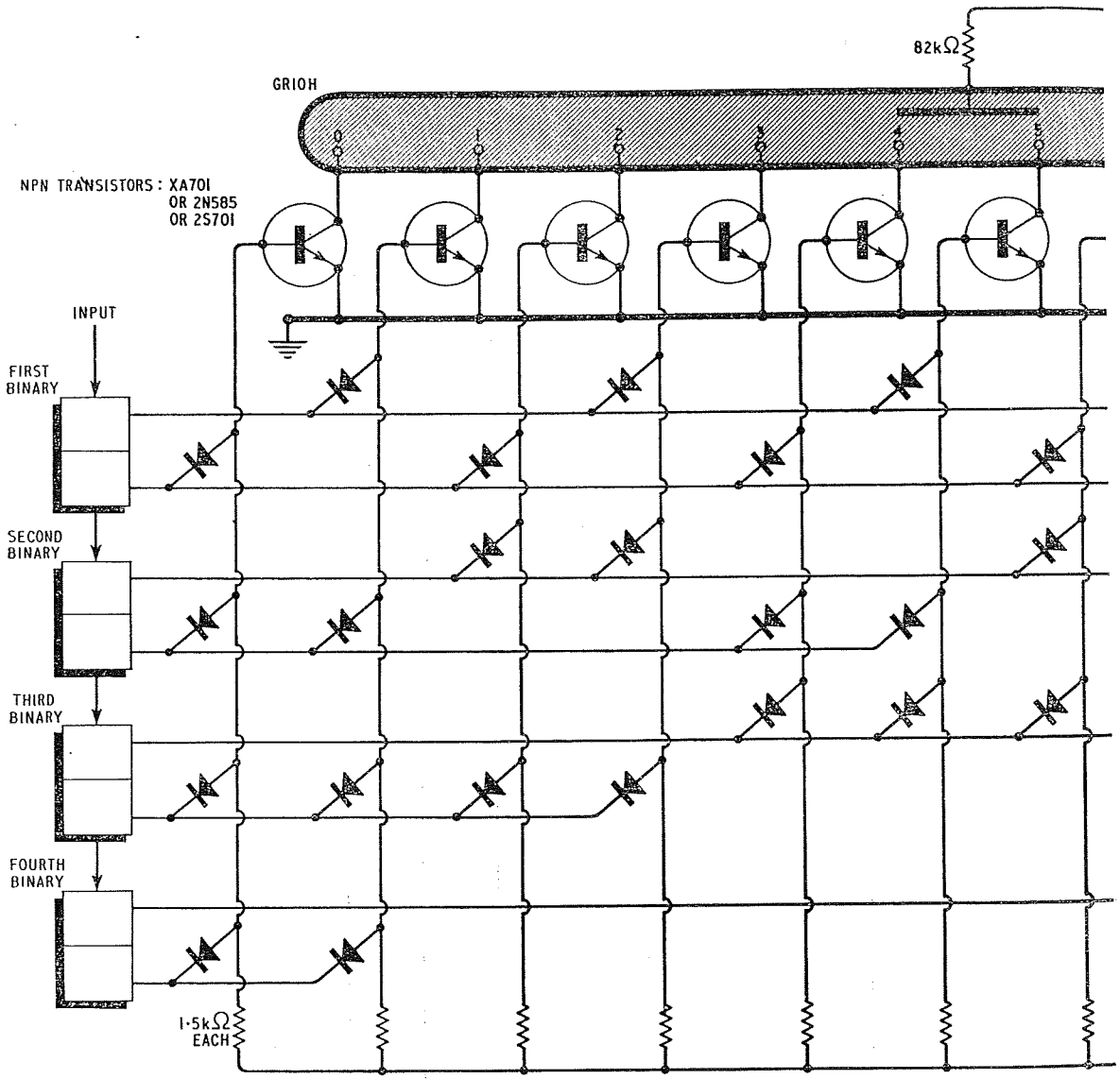
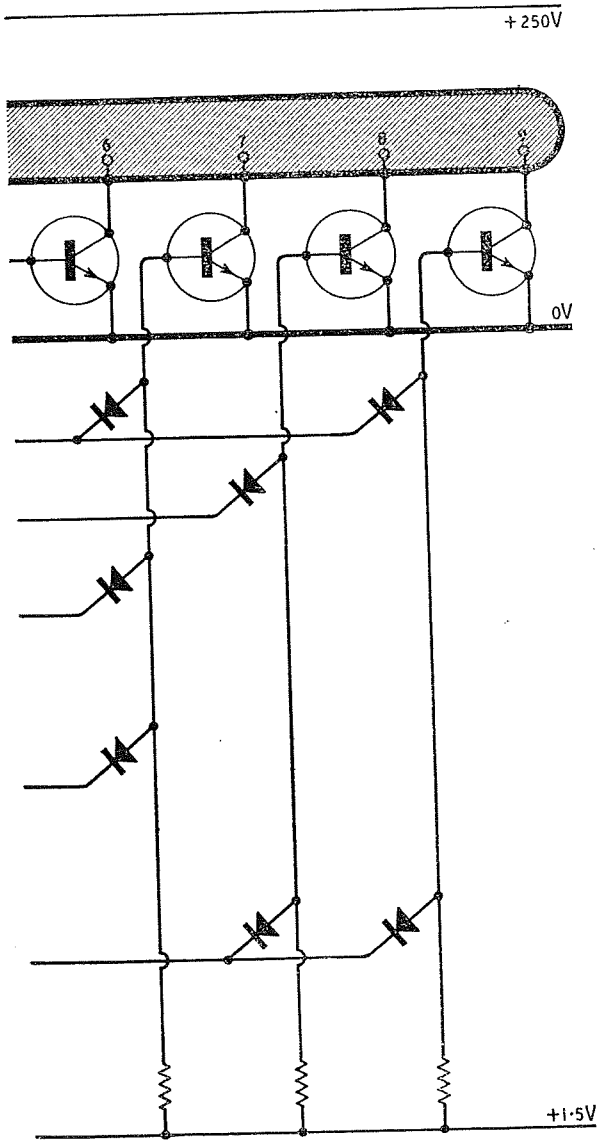


Fig. 8.16 The operation of a numerical indicator

8.1.6 10 Mc/s Decade

Transistors with cut off frequencies of the order of 300 Mc/s are suitable for use in saturated decade circuits at frequencies up to about 10 Mc/s. A circuit using germanium diffused mesa PNP 2G103 transistors is shown in Fig. 8.17[21]. This circuit counts to nine in the binary code and is then reset. The emitter follower $T3$ is included to ensure that the capacitance loading of the first binary is kept reasonably small. The output of $T3$ either switches the second or the fourth binary according to the state of the latter. When $T9$ conducts, the presence of D_5 ensures that the junction of D_4, D_5 and D_6 never becomes negative with respect to the output potential of the decade (−0.2 V). Positive pulses applied to the second binary are able to pass through D_4 or D_6 to switch the stage. When $T9$ is cut off, however, D_5 is reverse biased and its reverse leakage causes the potential at the junction of the three diodes to fall to −6 V, thus reverse biasing D_4 and D_6. No pulses can now pass from the first to the second binary.



tube from a transistor decade

D_{10} functions in a similar way to D_5. When $T8$ is conducting, pulses at the junction of D_{10} and D_{11} will switch the fourth binary, but when $T8$ is cut off, D_{10} and D_{11} are reverse biased and pulses from $T3$ will not be able to pass through D_{11} to switch the fourth binary. Nevertheless pulses from $T7$ will be able to switch the fourth binary, since they do not have to pass through D_{11}. The tenth pulse is thus gated from the first to the fourth binary.

The silicon gating diodes have forward and reverse recovery times of less than 4×10^{-9} sec. The maximum speed of the decade is, therefore, virtually the same as that of the first binary. Each conducting transistor passes a current of about 25 mA, but this cannot be appreciably reduced, however, without an increase in the resolving time taking place.

The meter readout is similar to that described for Fig. 8.13, but the readout resistor connected to the fourth binary must be one eighth of the corresponding resistor connected to the first binary, since a different feedback system is being employed. Each count produces 0.4 V into an open circuit or 70 μA into a short circuit. A meter with a full scale deflection of 630 μA or 3·6 V and scaled 0 to 9 is therefore required. The power consumed by the decade is less than 1 W.

Reversible transistor decade counters can be constructed if either output from the collectors of each binary can be used to trigger the next stage. The selection of the appropriate output can be made by transistors and this controls the direction of counting[22].

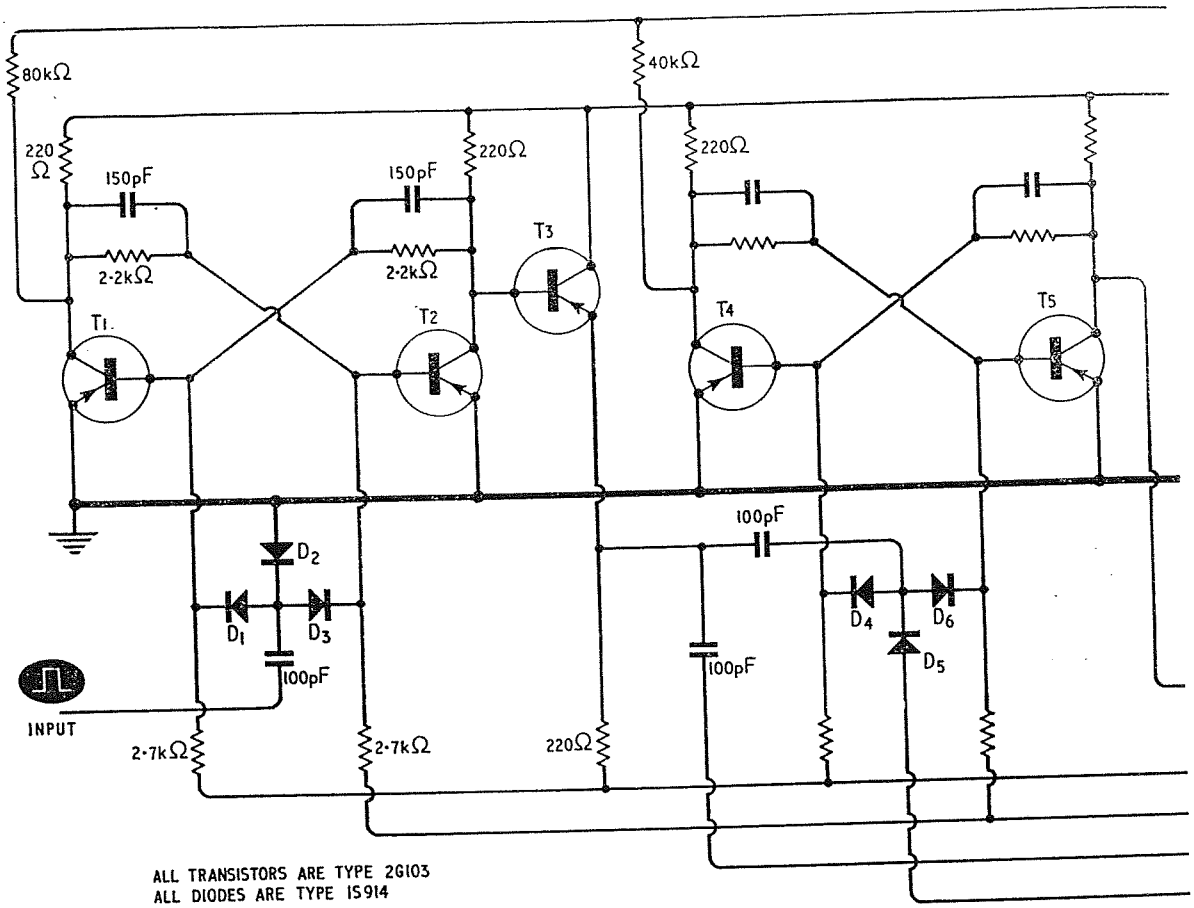
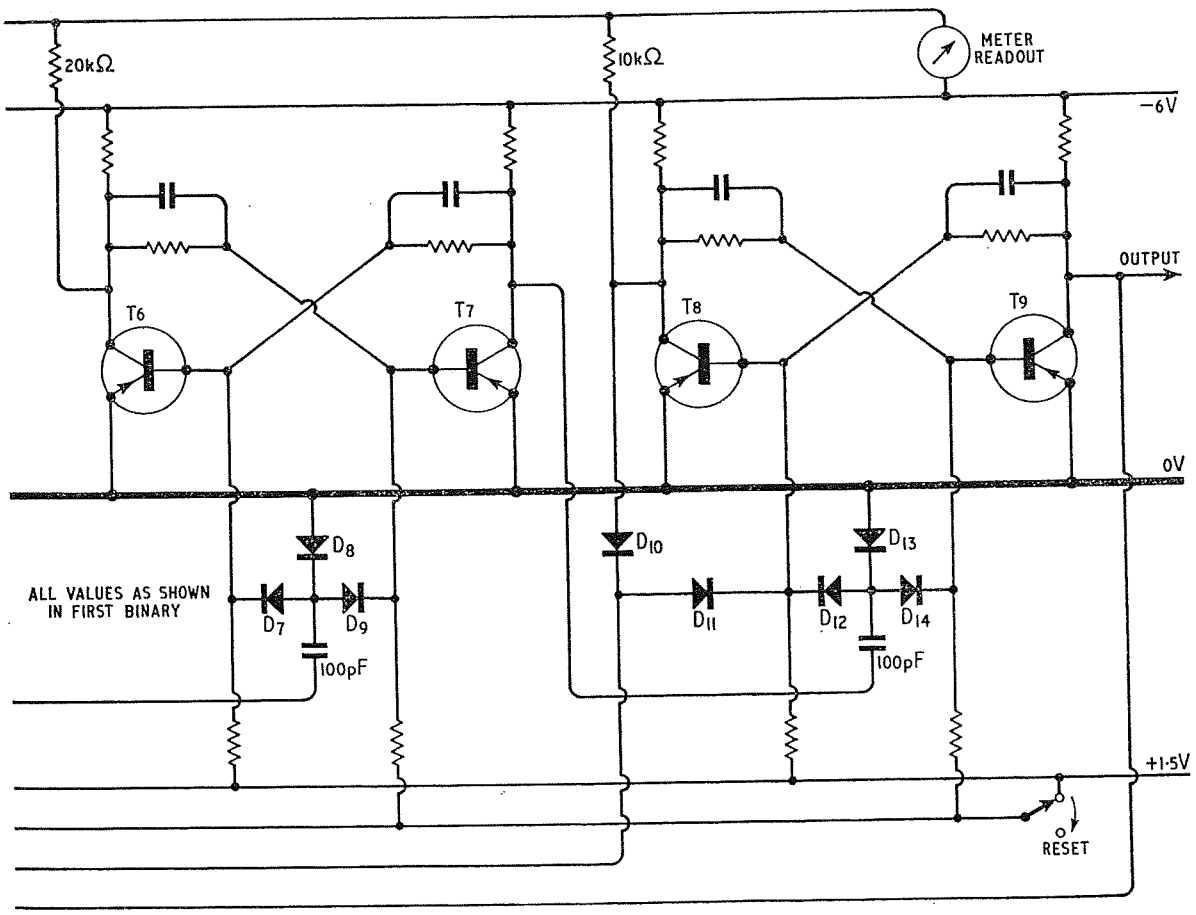

80kΩ
40kΩ
220 Ω
150pF
2·2kΩ
220Ω
T1
T2
T3
T4
T5
D1
D2
D3
D4
D5
D6
100pF
INPUT
2·7kΩ
ALL TRANSISTORS ARE TYPE 2G103
ALL DIODES ARE TYPE IS914

Fig. 8.17 A 10


20kΩ
10kΩ
METER READOUT
−6V
OUTPUT
T6
T7
T8
T9
0V
D8
D10
D13
ALL VALUES AS SHOWN IN FIRST BINARY
D7
D9
D11
D12
D14
100pF
100pF
+1·5V
RESET

Mc/s scaler.

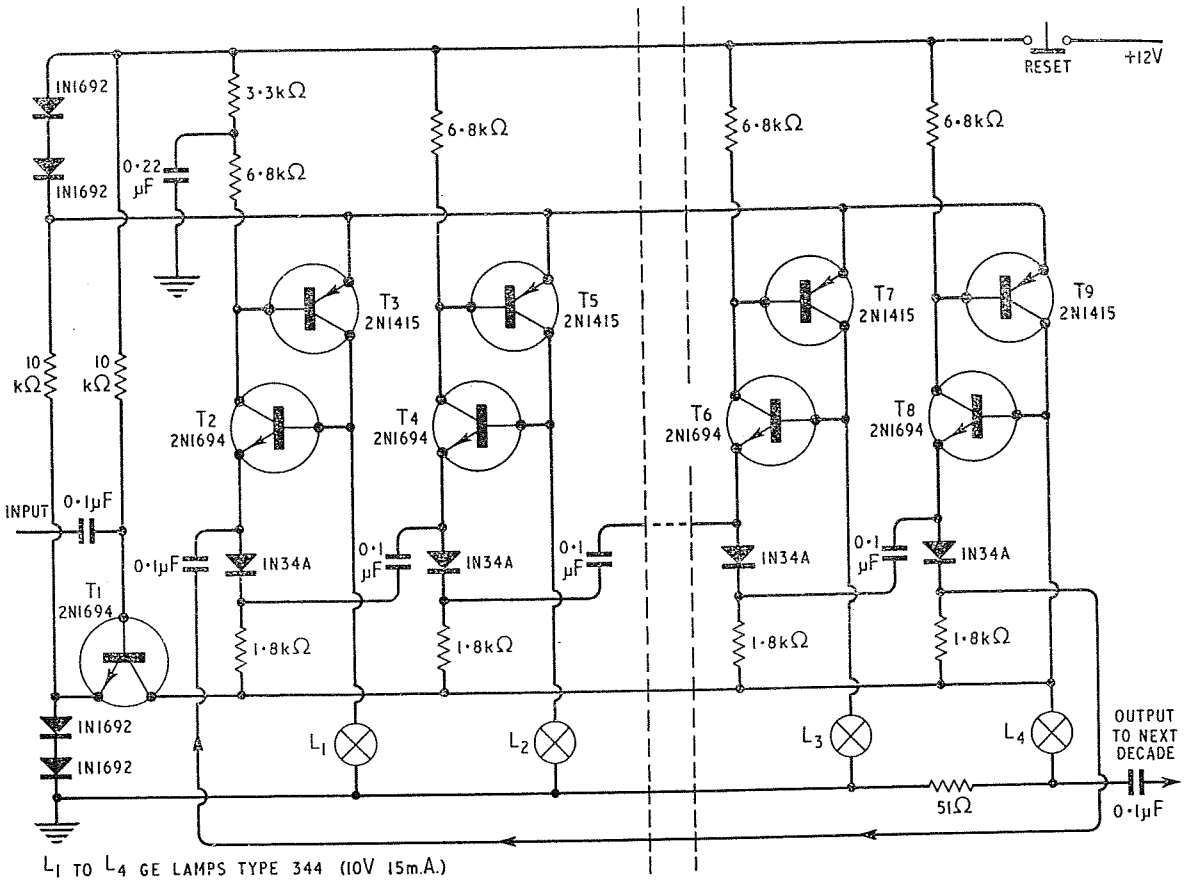


Fig. 8.18 A transistor ring counter

8.1.7 Ring Counter

A ring counter employing complementary symmetry bistable circuits is shown in Fig. 8.18[23]. Any number of stages may be included in the ring, only a very small current being drawn by the non-conducting stages. Readout is effected by means of filament lamps. The transistor $T1$ is a triggering transistor which amplifies the incoming pulses. When the reset button is pressed, the power supply is interrupted and the charge of the 0.22 μF capacitor in the circuit of the first stage ensures that this stage will conduct when the reset button is released.

8.1.8 Counters Employing a Diode Matrix

The Burroughs Corporation manufacture decimal counter modules ('BIPCO') type BIP-8001 which can count at up to 110 kc/s and provide visual readout by means of a 'Nixie' numerical indicator tube. The circuit of this type of counter is shown in Fig. 8.19[24]. The counter consists of a matrix of 90 diodes operating in conjunction with ten single transistor amplifiers and a bistable circuit containing two NPN transistors. The amplifiers are marked $A0$ to $A9$ in the circuit of Fig. 8.19. The inset shows the circuit of the $A0$ amplifier which provides the output pulse to the next decade. The circuits of the other nine amplifiers are similar, but the dotted components are omitted, since no output pulse is needed.

One of the ten amplifiers $A0$ to $A9$ is always conducting at any time. If $A1$ is conducting, the corresponding digit in the indicator tube will be glowing and the wire C from the cathode of the Nixie tube will be at a low potential. This wire is connected to amplifiers $A3$ to $A0$ inclusive via the diodes. The bases of the NPN transistors are, therefore, pre-

vented from becoming more positive than C and are cut off. When $A1$ is conducting, the binary will be in the state in which the wire marked A is at about earth potential and $A2$ will be cut off.

If an input pulse is used to switch the binary, the potential of the wire B will fall to about earth potential whilst that of wire A will rise to about 12 V. A1 is therefore cut off and $A2$ conducts. This results in the Nixie tube indicating the new count and the low potential of the wire D ensures that the amplifiers $A1$ and $A4$ to $A0$ are cut off. Each input pulse changes the state of the binary and causes the next amplifier to conduct. When the amplifier $A0$ conducts, an output pulse is produced which can be used to operate the next decade. This type of counter is effectively a ring of ten transistor amplifiers which are controlled by the diodes and the binary circuit. One of its main advantages is that the Nixie tube is driven directly from the ring without buffer amplifiers.

The negative going input pulses should have an amplitude of between 9 and 14 V and a duration of at least 2 μsec; their rise time should not exceed 0.5 μsec. The negative going resetting pulses should have an amplitude of at least 55 V and a minimum duration of 9 μsec. Electrical readout (up to 0.5 mA) may be obtained from the cathodes of the Nixie tube. When a cathode conducts, its potential falls from +55 V to +1 V nominal.

A similar module, the BIP-8002, can be used for reversible counting at frequencies of up to 20 kc/s.

8.1.9 Fast Scalers

Various circuit techniques have recently been developed to utilise suitable transistors for counting at frequencies up to at least 200 Mc/s[25]. Very high speed non-saturating binaries may be used or alternatively decade counters may be designed with gates connected in such a way that each binary reverses its state only once during the time several input pulses are applied to the circuit.

A 200 Mc/s scale of eight which may be followed by a 30 Mc/s decade scaler has been designed at Harwell[26]. This scaler has been developed from the non-saturating circuit of Chaplin and Owens[27] which was limited in frequency by the performance of the transistors which were available at that time. The binary circuits used employ a differentiating transformer instead of the usual capacitive coupling. A binary stage of this type is shown in Fig. 8.20[26]. D_2 is a 4.7 V zener diode.

When $T1$ is conducting about 6.7 mA passes to the emitter which assumes a potential of +0.2 V. The current flowing through D_3 produces a potential of 0.5 V across it. $T2$ is thus cut off.

A short negative going input pulse of at least 1 V amplitude will reduce the emitter potential of $T1$ so that it cuts off. A current now flows through D_4, D_2 and R_3 so that the base of $T2$ is at a potential of −0.5 V. At the end of the input pulse $T2$ will conduct before $T1$, since its base is more negative than that of $T1$. The flow of current through R_1 (7 mA) results in the common emitter potential becoming −0.3 V which prevents $T1$ from conducting.

A second input pulse reduces the common emitter potential so that $T2$ is cut off. A voltage is induced in the transformer when the current passing through it from $T2$ ceases. This voltage is arranged to have a duration somewhat longer than that of the input pulse and is applied to the base of $T1$ as a negative going pulse. $T1$ therefore commences to conduct at the end of the input pulse and the circuit returns to its first stable state. R_4 is used to critically damp the transformer voltage.

When $T2$ commences to conduct, the positive overshoot at its collector may be inverted by the transformer and used for triggering the succeeding stages. The step down ratio of the transformer increases the output current available for the operation of the succeeding stage. A transistor coupling amplifier is required when the resolving time of the circuit is reduced below 0.1 μsec, since the output pulse amplitude decreases with resolving time. No step down winding is then required and a smaller primary inductance may be used which helps to reduce the resolving time.

The transformers consist of two ferrite tubes with the wires passed through them. These components are small and the inductance may be varied by altering the type of ferrite. If a resolving time of 5×10^{-9} sec is required, 2N700 transistors may be used with a transformer consisting of two rods of Mullard FX1 361 ferrite each $^3/_8$ in. long. The

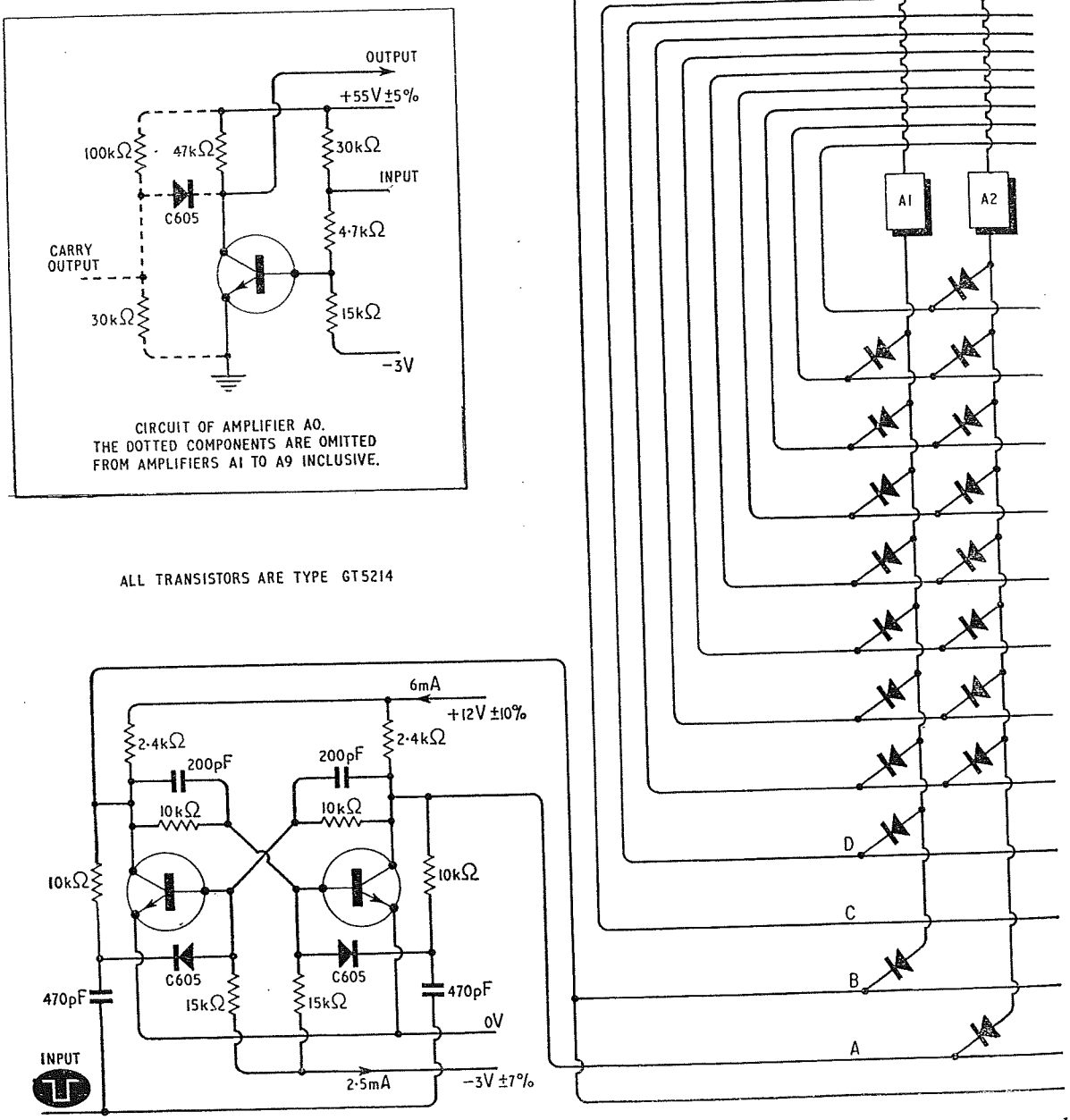
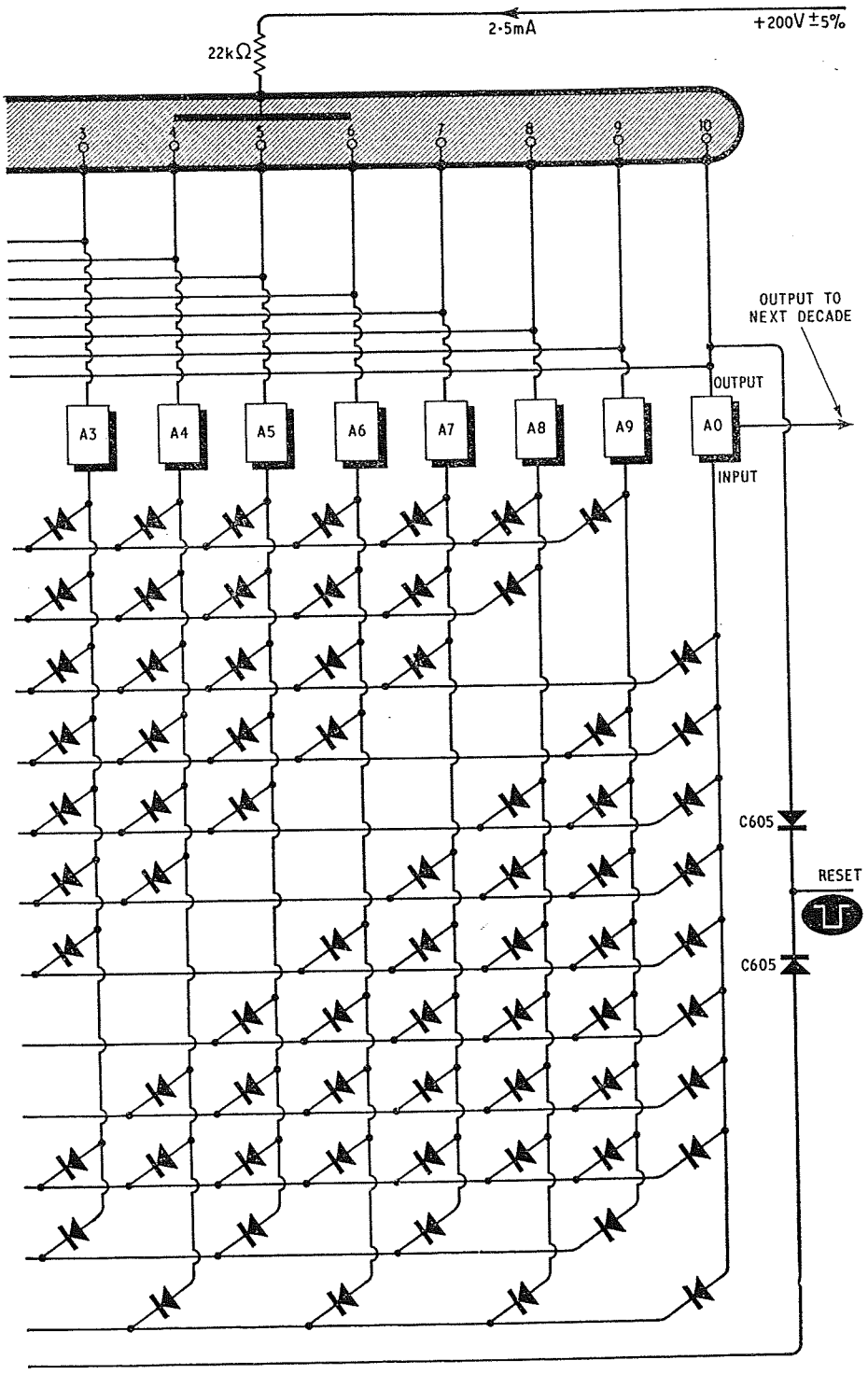


Fig. 8.19 The Burroughs



BIP-8001 decade counter

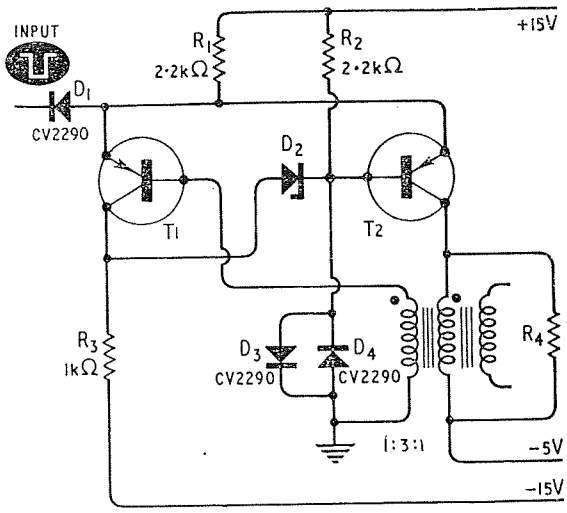


Fig. 8.20 A basic high speed binary circuit

transformer design should be varied according to the type of transistors used.

A 200 Mc/s scale of eight is shown in Fig. 8.21[26]. The first two binaries use 2N700 mesa transistors whilst the third binary can employ a 2N501 micro-alloy diffused transistor. *T*1, *T*5 and *T*8 are the coupling transistors. Circuits for a 30 Mc/s and a 3 Mc/s decade scaler constructed with the same type of binary circuit as Fig. 8.20 have been published[26].

8.1.10 Special Coding Systems

The maximum operating frequency of conventional types of transistor counters is limited to a value somewhat less than the maximum frequency of the first binary. However various systems have been devised in which no binary counts at a speed as

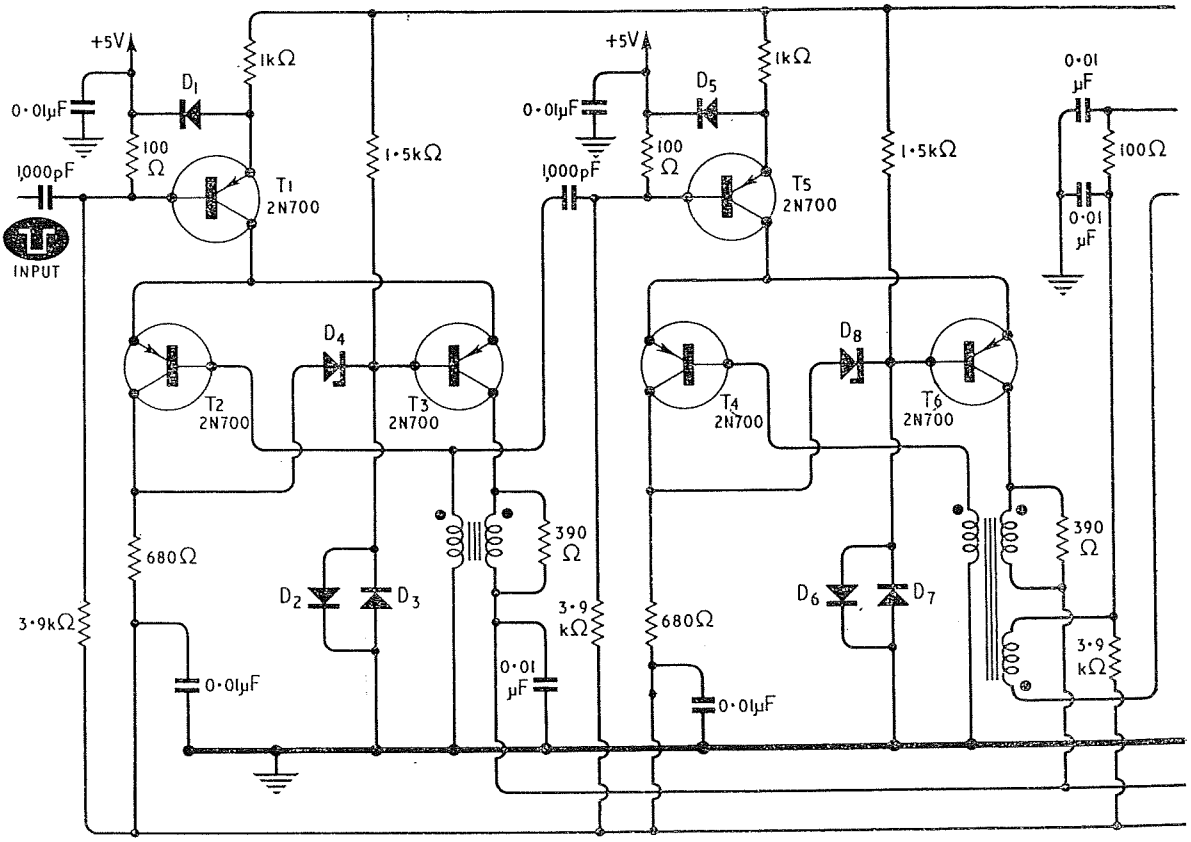


Fig. 8.21 A 200 Mc/s scale of eight. D_1, D_2, D_2, D_5, D_6, D_7, D_9, D_{10} and D_{11} are diodes CV2290; D_4, D_8 and D_{12} transistors; T7–T9

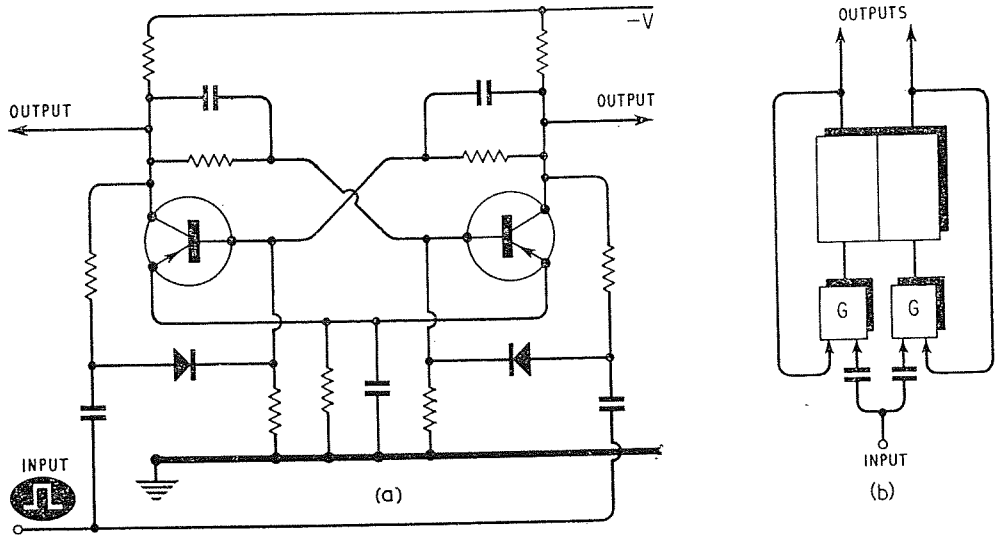
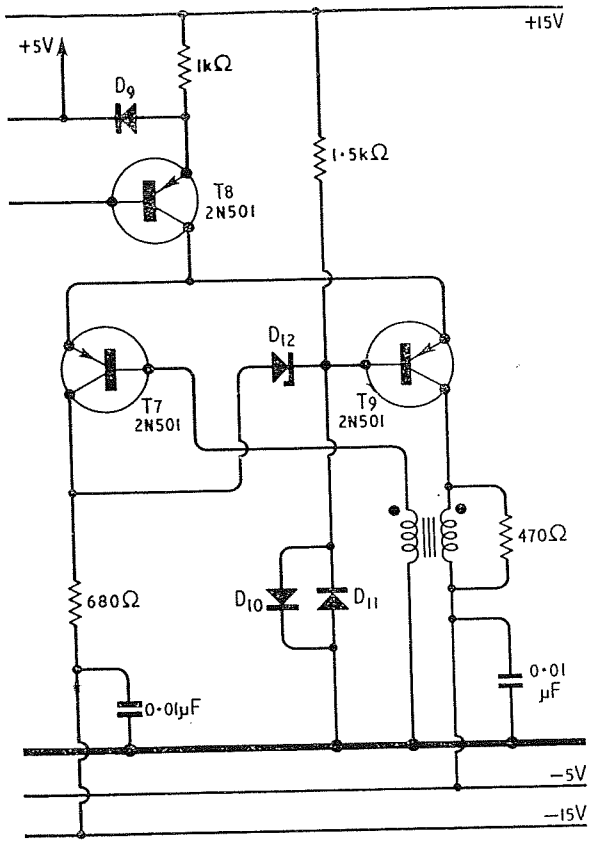


Fig. 8.22 A gated binary and its symbol



are 4·7 V Zener diodes (SX47); T1–T6 are 2N700 are 2N501 transistors

great as that of the input frequency. These types of counter use the state of the binaries to control gates which determine which binary will be switched by the next input pulse. Saturated binaries can be used in these type of circuits at input frequencies of up to about 200 Mc/s.

In order to show the functioning of such circuits, it is convenient to use the symbol shown in Fig. 8.22(b) to represent the binary of Fig. 8.22(a) with its diode gating circuits. Each gate feeds a transistor base and the collector potential of the same transistor is used to open or close this gate. If a transistor is in the cut off state, its collector applies a negative potential to the gate feeding its base and no pulses can pass to it. Positive going input pulses are gated to the conducting transistor which is thus cut off. Two outputs are available, but in normal cascaded binary circuits only one of them is used. In the circuits to be discussed the collector potentials of each binary are used to gate the input circuits of other binaries. The resolving time is determined more by the speed of the gating circuits than by the speed of the binaries.

An example of a counting circuit using a special coding system is shown in Fig. 8.23[28]. The positive going input pulses are fed to all gates, but a pulse will not be able to pass through a gate unless the collector of the transistor in the other binary to

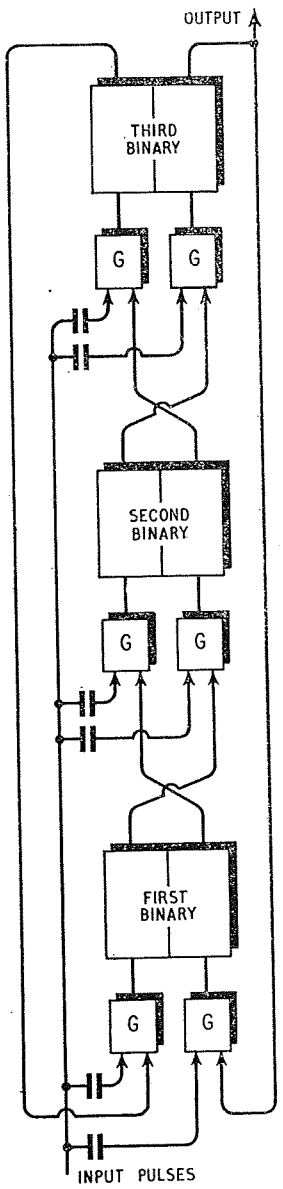


Fig. 8.23 A scale of six circuit

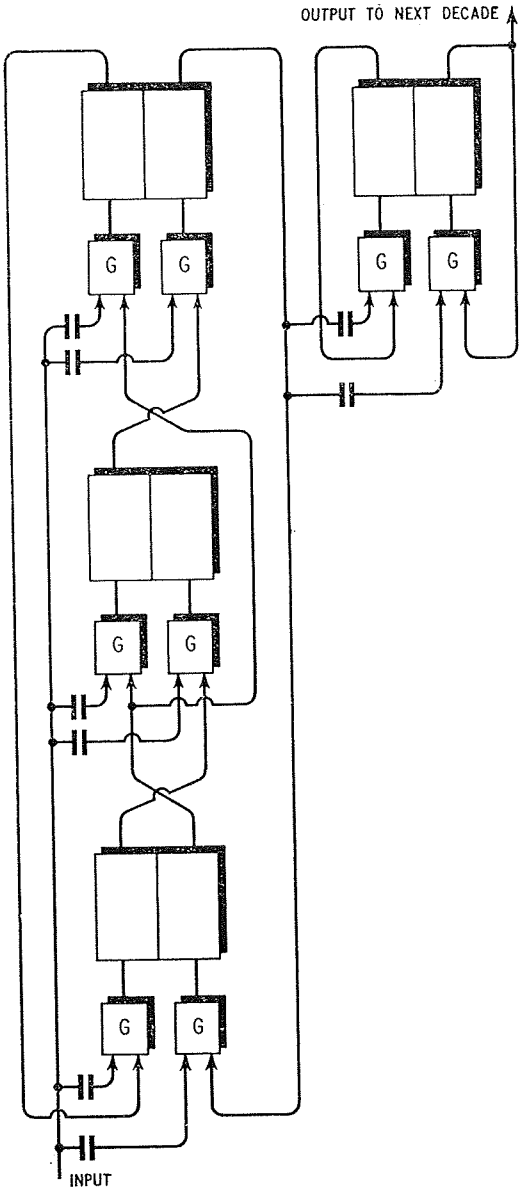


Fig. 8.24 A decade scaler

which the gate is connected is conducting. If a pulse passes through a gate, it will not switch the stage unless it passes to the side of the binary which is conducting.

In order to illustrate the cycle of operation, all of the binaries will be assumed to have been reset to the zero state in which the right-hand transistor is conducting. An input pulse applied to the circuit will be able to pass to the left-hand transistors of the second and third binaries, since their gates are connected to the conducting transistors in the previous stages, but no effect will be produced, as an input pulse will not affect a cut off transistor which is already in the state to which the input pulse would advance it. The input pulse can also reach the right-hand conducting transistor of the first binary because the gate feeding this transistor is connected to the conducting side of the third binary. The first binary is therefore switched. The gates feeding the left-hand side of the first binary and the right-hand sides of the second and third binaries are closed in the zero state.

When a second input pulse is applied to the circuit, it cannot affect the first binary, since it can reach only the non-conducting side of this stage via the right-hand gate. The switching of the first binary has, however, opened the gate which feeds the right-hand side of the second binary; the latter is therefore switched. The gate to the right-hand side of the third binary is now open and this stage will be switched by the third input pulse. The switching of the third binary opens the left-hand gate to the first binary so that the fourth input pulse switches the first stage back to zero. The fifth and sixth input pulses switch the second and third binary stages respectively back to zero. Thus after six pulses the whole counter has been reset. The coding for the operation of this type of counter is shown in Table 8.4.

Table 8.4

No. of Pulses	*State of the Binaries* 3rd	2nd	1st
0	0	0	0
1	0	0	1
2	0	1	1
3	1	1	1
4	1	1	0
5	1	0	0
6	0	0	0

It can be seen that each binary is switched only once for each three input pulses which are applied to the circuit. The system may be compared with a ring circuit, but the change of state travels around the ring twice instead of once per cycle as in standard ring counters.

The capacity of this type of counter is only $2n$ counts where n is the number of binary stages employed, but a normal binary counter has a capacity of 2^n counts. One method by which the same count capacity as a normal cascaded binary counter may be achieved and in which the speed of the first binary is halved involves the use of the Gray code[29] which is shown in Table 8.5.

Table 8.5

No. of Pulses	*State of the Binaries* 3rd	2nd	1st
0	0	0	0
1	0	0	1
2	0	1	1
3	0	1	0
4	1	1	0
5	1	1	1
6	1	0	1
7	1	0	0
8	0	0	0

The circuit of Fig. 8.24 is a decade scaler based on the circuit of Fig. 8.23[28]. The group of three binaries has been made into a scale of five by connecting the left-hand gates of the second and third binaries to the collector of the right-hand transistor of the first binary. At the fifth pulse the second and third binaries switch simultaneously. A binary circuit follows the scale of five so that the overall circuit forms a scale of ten.

Many high speed scalers are constructed on the principle of Fig. 8.23, but two additional binaries are used in the ring to make a scale of ten[30]. Such circuits may be called 'five binary decimal counters'. Each binary counts at only one fifth of the pulse

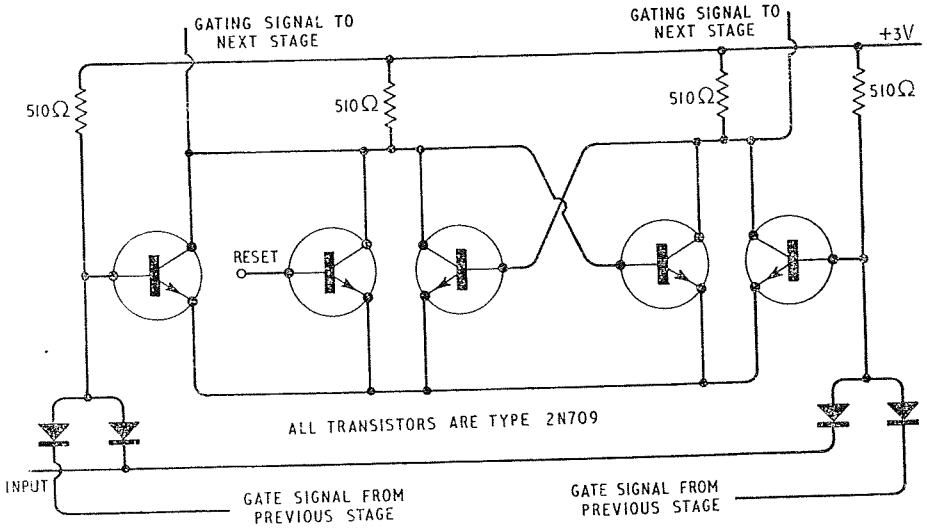


Fig. 8.25 An LLDL binary stage

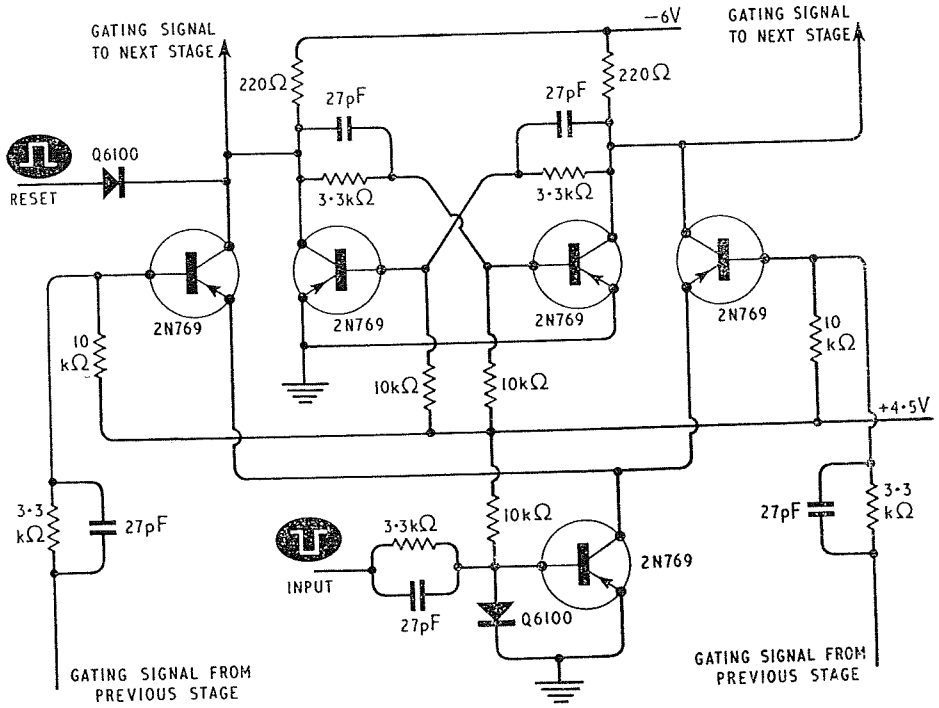


Fig. 8.26 A saturated binary stage for 100 Mc/s five binary decimal counting

input frequency, but one more binary is required in each decade than is employed in the circuit of Fig. 8.24. Five of the binary circuits shown in Fig. 8.25 may be used to construct a 100 Mc/s five binary decimal counter[31]. The connections are exactly similar to those of Fig. 8.23, but five stages are used in the ring. The circuit employs NPN 2N709 transistors which have a cut off frequency of 1,000 Mc/s in low level diode logic circuits.

A number of circuits have been published recently in which all transistor logic circuits are used in five binary decimal counters[31-33]. A saturated binary circuit designed for 2N769 transistors is shown in Fig. 8.26; it may be used in 100 Mc/s five binary decimal counters[32]. Both the gating and counting are performed by transistors.

The length of the input pulse which is used to operate a five binary decimal counter must be carefully controlled. It must be greater than the rise time of the gating circuit, but if it is too long, it may cause more than one binary to switch. The loading imposed by the circuit on the source of input pulses can be considerable, since both sides of all of the binaries are connected to the input.

Five binary decimal counters are normally constructed in a circle with the common input connection at the centre in order to minimise lead lengths. It is possible to obtain miniature encapsulated circuits containing several transistors and the use of such circuits enables higher operating speeds to be obtained, since the stray inductance and capacitance can be made very small. The use of five binary decimal counters enables high speed saturating scalers to be designed which have a much smaller power dissipation than non-saturating scalers. This type of circuitry is a great aid to miniaturisation.

8.2 SCALERS USING FOUR LAYER SWITCHING DEVICES

A number of semiconductor devices which have a four layer PNPN structure are being marketed under various names including 'Trigistor', 'Transwitch', 'Four Layer Diode', 'Shockley Diode', 'Trinistor', 'Silicon Controlled Rectifier', 'Dynaquad', 'Silicon Controlled Switch', etc. In all types connections can be made to the two layers at each end of the PNPN structure, but some types are three terminal devices in which a current can be passed to one of the inner layers. The silicon controlled switch is a four terminal device with connections to all of the four semiconductor layers. A connection made to the P type inner layer is known as a P gate and a connection to the N type inner layer as an N gate.

PNPN devices are very suitable for use in ring counters, since they possess somewhat similar properties to cold cathode tubes, but have the advantages that they can operate at much higher speeds and are much more efficient.

In a four layer diode, connections are made only to the two layers at each end of the device. A single four layer diode has two characteristic stable states. In one state the impedance is about 100 MΩ whilst in the other state it is only a few ohms. When a small voltage is applied across it, the diode is in its high resistance state but (like a neon diode) it can be switched into its conducting state by the application of a voltage above a certain minimum value; this minimum value is known as the 'breakover' voltage (V_{b0}). In some devices the switching occurs in 0.1 μsec.

The diode can be returned to its high resistance state by reducing the current passing through it below a certain value which is known as the holding current. The time taken is not usually much less than 1 μsec, since stored charges must be removed before the switching operation is completed.

If the PNPN device is a three or four terminal one, it can be operated in a similar way to a trigger tube. The voltage applied across the whole device is normally somewhat less than the breakover voltage, but a suitable current pulse applied to one of the inner layers will cause switching to the low resistance state to take place. The device will remain in the low resistance state until either the main anode to cathode voltage is removed or until a pulse of opposite polarity is applied to one of the inner layers. A negative pulse applied to a P gate or a positive pulse applied to an N gate can be used to stop conduction. Trigger tubes do not possess a comparable property.

The form of the characteristic curve of a PNPN device is shown in Fig. 8.27. The high impedance

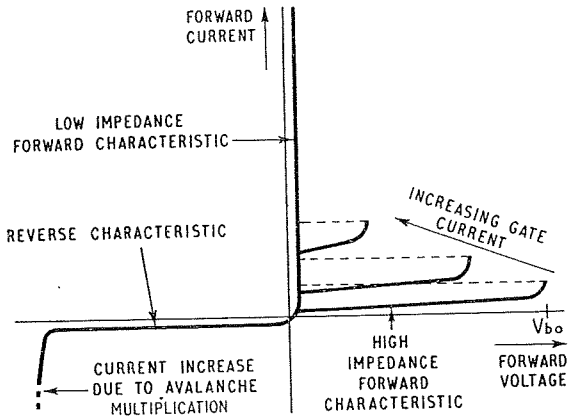


Fig. 8.27 The characteristics of a PNPN device

forward characteristic is almost a mirror image of the reverse characteristic, but soon after the curved part of the forward characteristic is reached, the device will switch to the low impedance state by following the dotted line. It can be seen that as the gate current increases, the breakover voltage decreases. PNPN devices can be produced with a low reverse impedance.

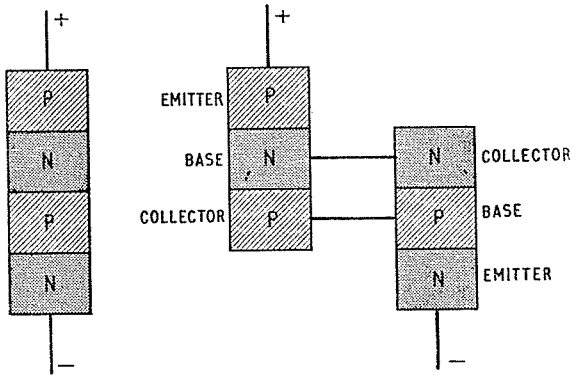


Fig. 8.28 A PNPN device is equivalent to a PNP and an NPN transistor connected as shown

Fig. 8.28 shows that a PNPN device can be regarded as a PNP and an NPN transistor connected as in the bistable circuit of Fig. 8.8. The collector of the one transistor is the same layer as the base of the other. Forward biasing occurs when the applied voltage has the polarity shown. The two outermost junctions are forward biased, but the centre junction is reverse biased. The whole device therefore has a high impedance until the potential across it is increased to the point at which avalanche multiplication occurs at the centre junction. This effect may be compared with the avalanche effect in gas filled tubes. If a positive potential is applied to the inner P layer or a negative potential to the inner N layer (each of which is the base of one of the transistors), the current will be amplified by normal transistor action and switching to the low impedance state will occur. The gate current effectively lowers the breakover voltage.

8.2.1 Circuits Using PNPN Diodes

A simple ring counter using four layer or Shockley diodes is shown in Fig. 8.29[34]. The four layer diodes are marked $4D_1$, $4D_2$, etc. The diode $4D_1$ is a triggering diode which amplifies the input pulse; it is not part of the ring. Any number of additional stages may be included between the dotted lines.

When the supply voltage is first applied to the circuit, one of the four layer diodes will switch to its low resistance state. It will then pass a current which produces a large enough voltage drop across R_2 and R_3 to prevent any other diode in the ring from conducting. The value of R_1 is large enough to prevent $4D_1$ being switched to the conducting state, since this resistor will not pass the holding current with the supply voltage specified.

A negative pulse of 16 to 36 V in amplitude applied at the junction of $4D_1$ and D_1 will cause $4D_1$ to be momentarily switched to the conducting state and its anode voltage to fall virtually to earth potential. This negative voltage pulse is coupled through C_1 to the H.T. supply line in the ring counter, the potential of which falls also. The stage which was conducting is thus switched to its high resistance state. The coupling capacitor in the anode circuit of the conducting stage has charged during the conduction period and, as the potential of the H.T. supply line rises again, the potential across this capacitor is added to the supply potential so that the succeeding stage is switched. Each input pulse thus causes the state of conduction to advance one place in the ring.

The diode $4D_1$ may be a 4D40-10 with a nominal switching potential of 40 V, whilst the other four

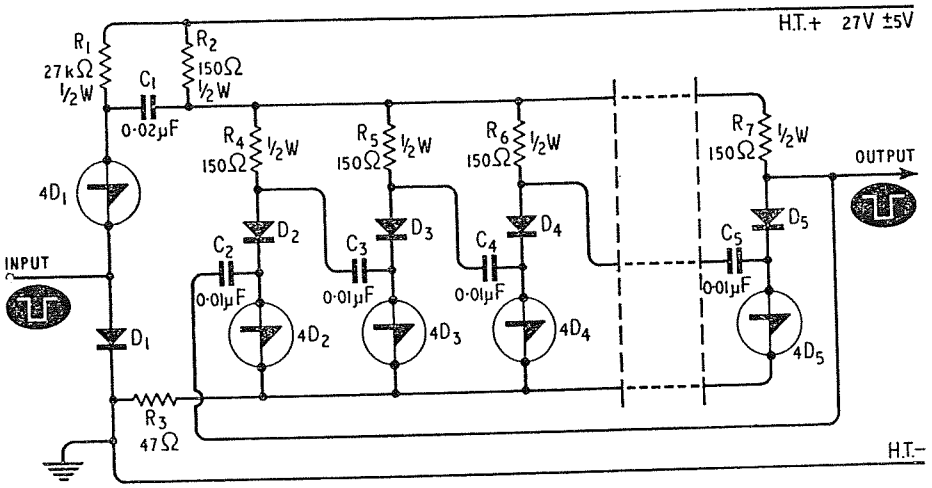


Fig. 8.29 A 2 kc/s ring counter using four layer diodes

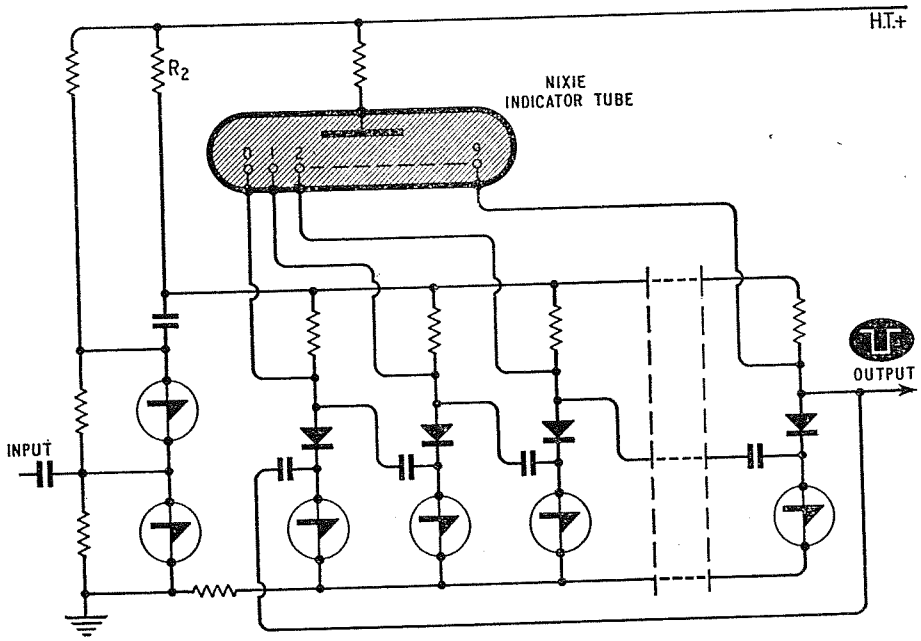


Fig. 8.30 Nixie tube readout from a Shockley diode ring counter

layer diodes may be type 4D20-10 which have a switching potential of 20 V. Both types have holding currents of 10±5 mA. The silicon diodes D_1 to D_5 may be type 1N461 or similar. If a positive going output pulse is required, it may be obtained by placing a resistor of low value in the cathode circuit of the final stage. Somewhat higher counting speeds may be obtained if a transistor trigger stage is used instead of D_1, $4D_1$ and R_1.

The circuit may be modified so that it can drive a 'Nixie' numerical indicator tube as shown in Fig. 8.30[35]. This tube requires an ignition potential of at least 250 V and R_2 must therefore be large so that only one stage of the ring conducts at any time. The diode D_1 of Fig. 8.29 must be replaced with a four layer diode and resistors should be placed in parallel with the four layer triggering diodes to divide the voltage equally between them.

A similar circuit has been designed for reversible counting in which two four layer diodes are used in each stage[36]. Circuits for use at 20 kc/s with neon tube readout have also been published[37].

8.2.2 Three Terminal Devices

The Trigistor is a silicon PNPN device with a connection to the inner P layer (P gate). Trigistors type 3C30 may be used in ring counters of the type shown in Fig. 8.31 for operation at frequencies up to at least 10 kc/s[38]. The input is maintained at a quiescent potential of +10 V which falls to +5 V during the pulse. If $T2$ is conducting, the upper (anode) side of D_2 will be at +10 V and the negative going input pulses will be able to pass through D_2 to $T2$. If $T2$ is initially conducting, it will be switched to its non-conducting state by an input pulse. When $T2$ is conducting, the anode of the diode D_3 will be at about earth potential. D_3 will therefore be reverse biased, since the potential of the input line is always at least 5 V positive with respect to earth (although the pulse itself is negative going). Therefore each Trigistor except the one following the conducting stage will receive a 'turn off' pulse each time an input pulse is applied. When a stage is switched off, the resulting positive going pulse is coupled by a capacitor to the gate electrode of the next stage which is thus switched to conduction.

A circuit which employs germanium ATZ10 transistors with an OC41 driver stage is shown in Fig. 8.32[39]. The load resistors are arranged so that only one stage can conduct at any time. When the OC41 driving transistor is switched to conduction, its emitter current reduces the current available to the stages in the ring which are thus switched off. When the conducting stage is switched off, it passes a positive going pulse through the coupling capacitor to the base of the succeeding stage; the latter is turned on at the end of the input pulse. The maximum frequency is about 30 kc/s.

Ring circuits using silicon P gate devices for frequencies up to 100 kc/s[40] have been designed,

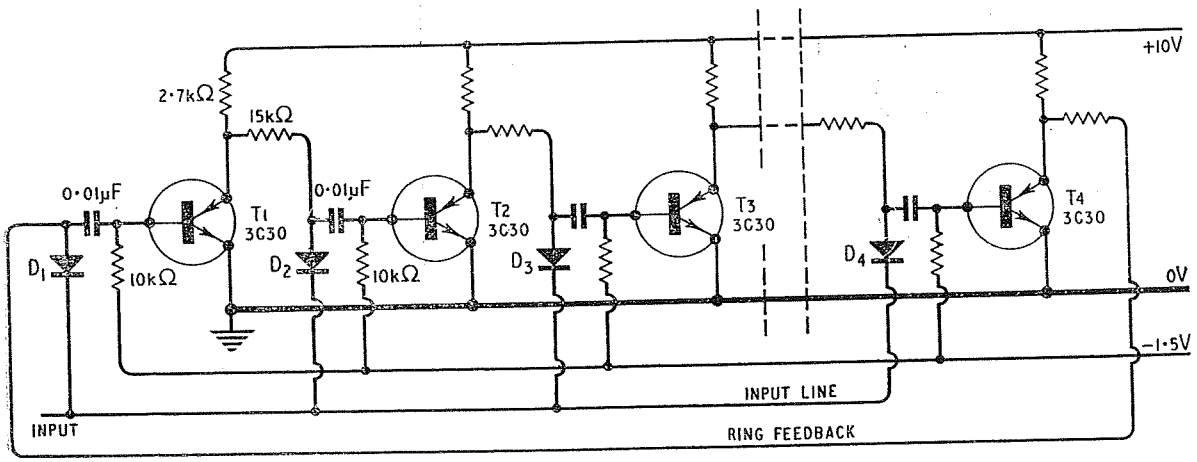


Fig. 8.31 A Trigistor ring circuit. Component values are shown in the first stage

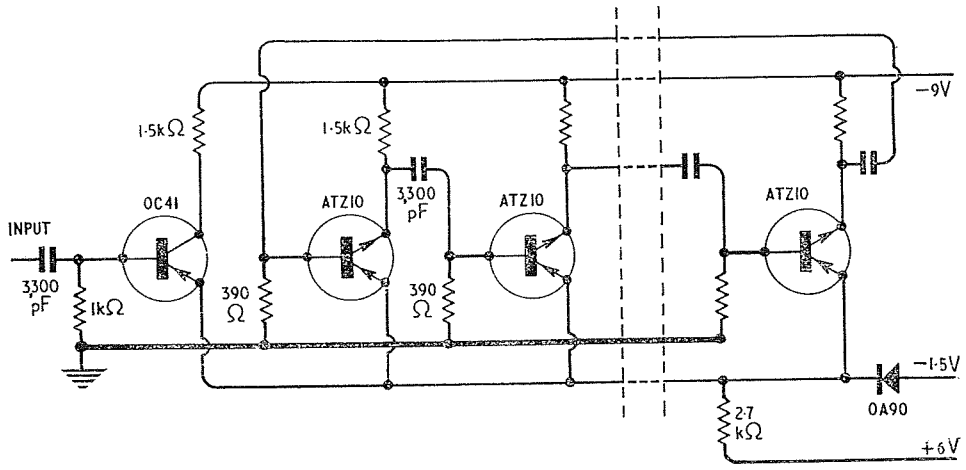


Fig. 8.32 A 30 kc/s ring circuit

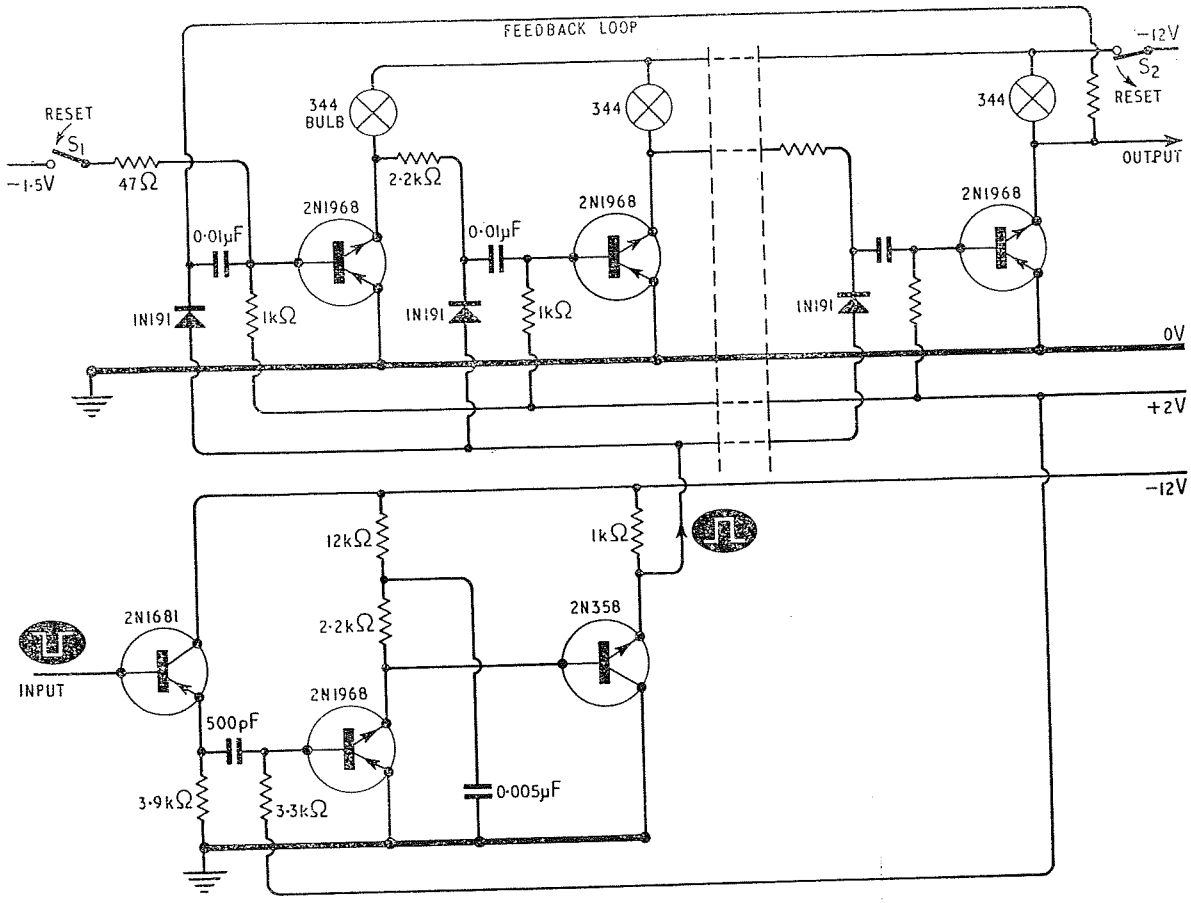


Fig. 8.33 A 20 kc/s Dynaquad ring counter

controlled rectifiers (also P gate) can ıg circuits for switching many amps at up to at least 1 kc/s[41].

alled 'Dynaquad' is a germanium PNPN ıth a connection to the inner N layer (N may be used in the type of ring counter sho. in Fig. 8.33[42]. The input pulses are fed into a 2N1681 emitter follower and the low impedance output from this stage is used to operate a 2N1968 Dynaquad monostable circuit which provides pulses of an 8 μsec duration. These pulses are directly coupled into a 2N358 NPN emitter follower which provides a low impedance output for the ring circuit. The positive going pulses can switch off a conducting stage, since Dynaquads have N gates. When a conducting stage is turned off, a negative pulse is formed which is used to switch the next stage to conduction. The 344 indicator lamps are rated at 10 V, 14 mA. The maximum frequency is about 20 kc/s.

The circuit may be reset by first momentarily opening S_2; this cuts off the power supply and turns all of the Dynaquads off. If S_1 is now closed for a moment, the negative current passing to the N gate of the zero Dynaquad will switch it to the low resistance state.

8.2.3 The Silicon Controlled Switch

The symbol for the four terminal silicon controlled switch is shown in Fig. 8.34. G_A is the N gate and G_C is the P gate. G_A is the layer next to the anode. These switches may be used in ring circuits of the

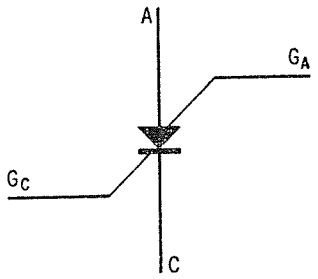


Fig. 8.34 The symbol for the silicon controlled switch

type shown in Fig. 8.35[23]. D is a zener diode with a working voltage of between 3 and 6 V.

The 4.7 kΩ anode resistor is chosen so that only one stage can conduct at any time. A positive going input pulse of about 10 μsec duration will cause the NPN input amplifier, $T1$, to conduct and this will reduce the potential of the common anode line so much that the conducting silicon controlled switch will be turned off. This results in a positive going pulse being formed at the anode gate which can be fed to the cathode gate of the succeeding stage and the latter is thus switched to the low resistance state. When the final stage is switched off, the common anode potential rises until the zero stage is turned on by the current passing through the zener diode. This circuit has the advantage that it is automatically set to zero when the power supply is first applied.

8.3 TUNNEL DIODE COUNTING CIRCUITS

The operation of the tunnel diode, unlike that of the transistor or the PNPN device, does not depend on

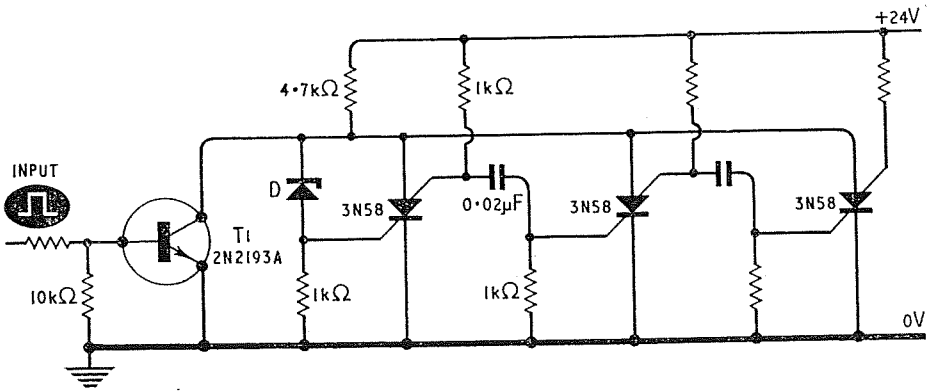


Fig. 8.35 A silicon controlled switch ring counter

the relatively slow diffusion of minority carriers across a field free region, but utilises the passage of majority carriers at a high velocity across a narrow junction. Transit time effects are therefore negligibly small and the tunnel diode is capable of operating at very high speeds. The switching time is a function of the junction capacitance and the negative resistance. Tunnel diodes can operate at a much smaller power than transistors and are ideal for use in miniature equipment. The design of tunnel diode circuits is simplified by the fact that the spread of some of the parameters can be made much smaller than in the case of transistors.

The tunnelling effect in semiconductors is a fairly recent discovery[43] and it is probable that new ways of using tunnel diodes in counting circuits will be developed in the future. Many different types of tunnel diode counting circuits can be constructed, but at the moment they are not very widely used. One of

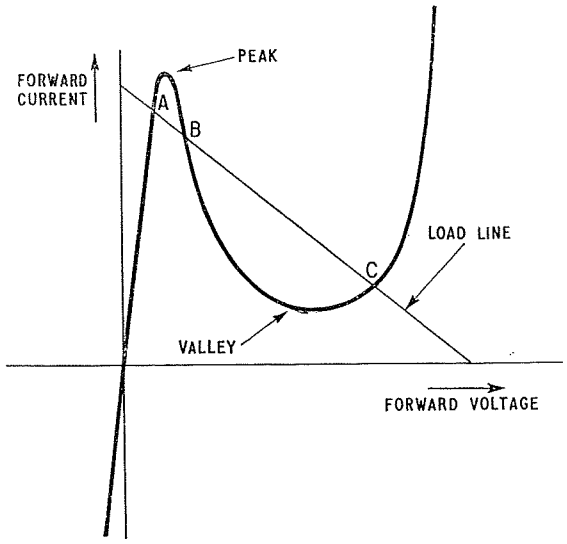


Fig. 8.36 The tunnel diode characteristic curve

the main difficulties being encountered is that of cascading tunnel diode circuits, since a tunnel diode does not provide a very suitable current source for driving a succeeding tunnel diode circuit. For this reason tunnel diodes are often used with transistors. Tunnel diodes lack the flexibility of most other active components because they have only two connections.

The characteristic curve of a tunnel diode is shown in Fig. 8.36. As the voltage applied across the diode rises, the current first rises to a maximum, then falls to the valley region and finally rises again. The diode exhibits a negative incremental resistance in the section of the curve in which the current decreases as the voltage increases. If the tunnel diode is connected to a load resistor which has a value somewhat greater than the negative resistance of the diode, a supply voltage can be chosen which will enable the load line to cut the characteristic in three places as shown in Fig. 8.36. The point B in the negative resistance region is unstable, but the circuit can be switched from the stable low voltage state at A to the stable high voltage state at C if a pulse is applied to increase the voltage across the diode. A pulse of the opposite polarity will switch the operating point back to A. A single tunnel diode can, therefore, be used as a bistable circuit if pulses of alternating polarity are available.

8.3.1 Bistable Circuits

A tunnel diode bistable circuit which can be operated from input pulses of constant polarity is shown in Fig. 8.37. This type of circuit is known as a Goto counter. The supply voltage is chosen so that only one of the diodes can be in its high voltage state at any time. The difference between the currents taken by the diodes passes through the inductance L. A positive going input pulse of suitable amplitude will switch the diode which is in the low voltage state to the high voltage state. The current passing through the inductance then falls and a voltage is induced across it which is of the correct polarity to switch the

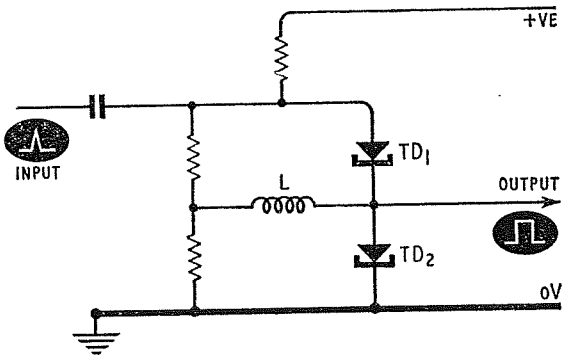


Fig. 8.37 A Goto binary circuit

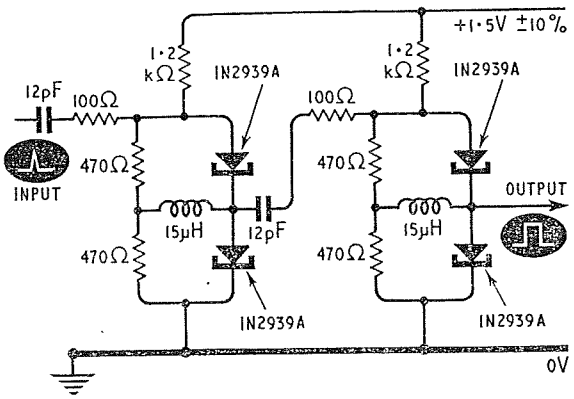


Fig. 8.38 A scale of four circuit using Goto binaries

other diode from the high to the low voltage state. A second input pulse will return the circuit to its initial state by a similar process.

A practical scale of four circuit for use at frequencies up to 10 Mc/s is shown in Fig. 8.38[44]. The input pulses to the 1N2939A tunnel diodes should have an amplitude of 0.5 to 0.7 V and a duration of 1/100 μsec at 10 Mc/s. The output pulses have an amplitude of 0.4 V. A similar circuit using two directly coupled tunnel diode bistable circuits has been published which will operate at frequencies up to 200 Mc/s[45].

Direct coupling of Goto counters is not always very satisfactory and there is some advantage is the use of transistor coupling circuits. The Goto circuits may be used with carry gates for high speed counting as shown in Fig. 8.39(a)[46]. Any counter stage will not receive an input pulse unless all of the previous carry gates are open. A carry gate will not be open if the Goto circuit to which it is connected is in the zero state. Fig. 8.39(b) shows the basic circuit of a carry gate using two NPN transistors. The output from the Goto circuit controls the current passed by $T1$ and this transistor is coupled to $T2$ so that the latter is either saturated or cut off. If it is saturated there is effectively a short circuit between its emitter and collector and the trigger pulse is propagated to the succeeding stages without any more delay than that caused by the wiring, since the pulses do not have to pass through any of the preceeding binaries. Eight successive carry gates may cause a delay of about 10^{-9} sec. If a Goto circuit is in its zero state, $T2$ of the corresponding carry gate will be cut off and the input pulse will not be able to pass to the succeeding stages.

The first input pulse cannot pass through the left-hand carry gate of Fig. 8.39(a), since the Goto circuit shown beneath this carry gate is in its zero state. However, this Goto binary will be switched by the input pulse so that a count is registered. The switching of this binary opens the first carry gate. The second input pulse will switch the first Goto circuit to zero and will pass through the first carry gate to switch the second Goto binary. However, the second carry gate is closed, so the pulse cannot pass to any other stages. A binary count of two is thus registered. The third input pulse can switch only the first binary, since the first carry gate is closed. Thus a binary count of three is registered. The fourth pulse switches the first binary to zero,

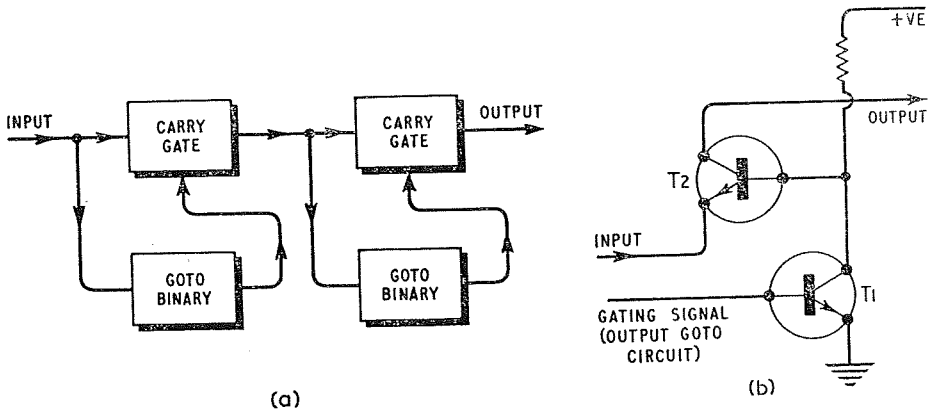


Fig. 8.39 Fast counting with transistor gated Goto binaries

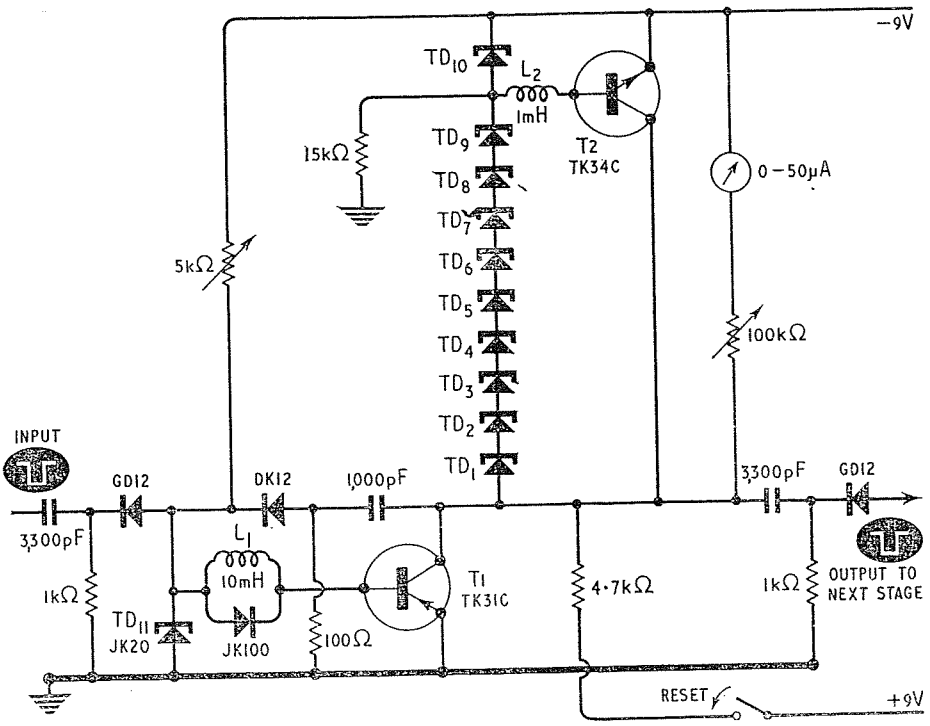


Fig. 8.40 A tunnel diode current switched decade

passes through the first carry gate to switch the second binary to zero and passes through the second carry gate to provide an output pulse for the operation of any succeeding binaries. Thus the system counts on the normal binary scale.

8.3.2 Tunnel Diode Chain Circuits

A number of tunnel diodes may be connected in series and used in a circuit which enables each input pulse to switch one diode from the low to the high voltage state. When all of the diodes have been switched, a transistor is usually used to return them all to the low voltage state.

In one type of chain circuit the tunnel diodes used are carefully selected so that their peak currents vary over a range of values. For example, they may range from 5 to 10 mA in increments of 0.5 mA. In this case a constant bias of less than 5 mA but greater than the valley current of any diode would be passed through the chain. When the diodes are all in their low voltage state, the circuit will be at zero. The input consists of a current of increasing amplitude which passes through the tunnel diode chain and which switches the first diode and then falls to zero. The next input pulse switches the diode with the next higher peak current.

A decade counter of this type is shown in Fig. 8.40[41]. It employs eleven tunnel diodes and provides meter readout. The tunnel diodes TD_1 to TD_{10} inclusive are selected for increasing peak currents from 6 to 10 mA. The JK100 is a backward diode. The input pulses should be negative going 5 mA current pulses with a maximum duration of 10 μsec The input impedance depends mainly on the impedance of the input diode; it may be as low as 30 Ω. The circuit can count at frequencies up to about 1 Mc/s, the limiting factor being the rapidity with which the resetting operation can be carried out.

The input pulses are used to switch the tunnel diode TD_{11} to its high voltage state. The change of potential at the cathode of this diode drives an exponentially rising current through the inductance L_1 into the base of the TK31C transistor amplifier, $T1$. The output from this transistor passes through the diode chain TD_1 to TD_{10}. When the diode with

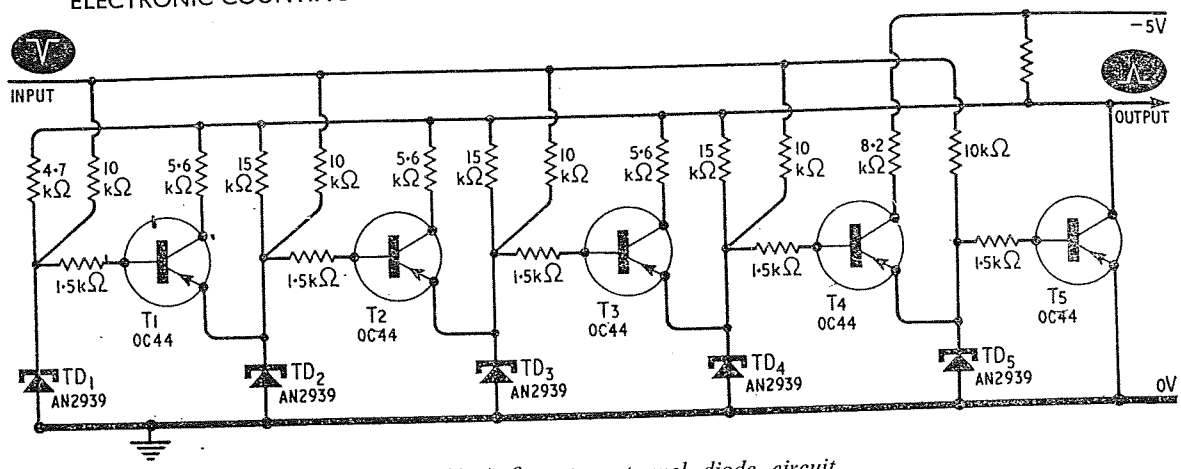


Fig. 8.41 A five stage tunnel diode circuit

the lowest peak current changes its state, the anode of TD_1 becomes more positive and a pulse is applied through the DK12 diode to return TD_{11} to its low voltage state. L_1 is bypassed by a backward diode to obtain a high speed resetting action. TD_{10} has the highest peak current and is therefore the last diode to change its state. When it is switched by the tenth input pulse, a positive pulse is applied to the base of the NPN transistor $T2$ which therefore conducts and effectively short circuits the tunnel diode chain. Thus the ten diodes are reset to their low voltage state. The 15 kΩ resistor connected between earth and the junction of TD_9 and TD_{10} ensures that TD_{10} is the last diode in the chain to be reset. L_2 delays the resetting operation until the current in $T1$ has ceased to flow. The reset pulse from $T2$ is also used as the output but is prevented from reaching TD_{11} by the DK12 diode.

In another type of circuit[48] voltage input pulses are applied through a capacitor to the tunnel diode chain and the pulse amplitude is chosen so that a pulse can cause only one diode to switch. The diodes are not specially selected and normally the diode with the least junction capacitance will switch first.

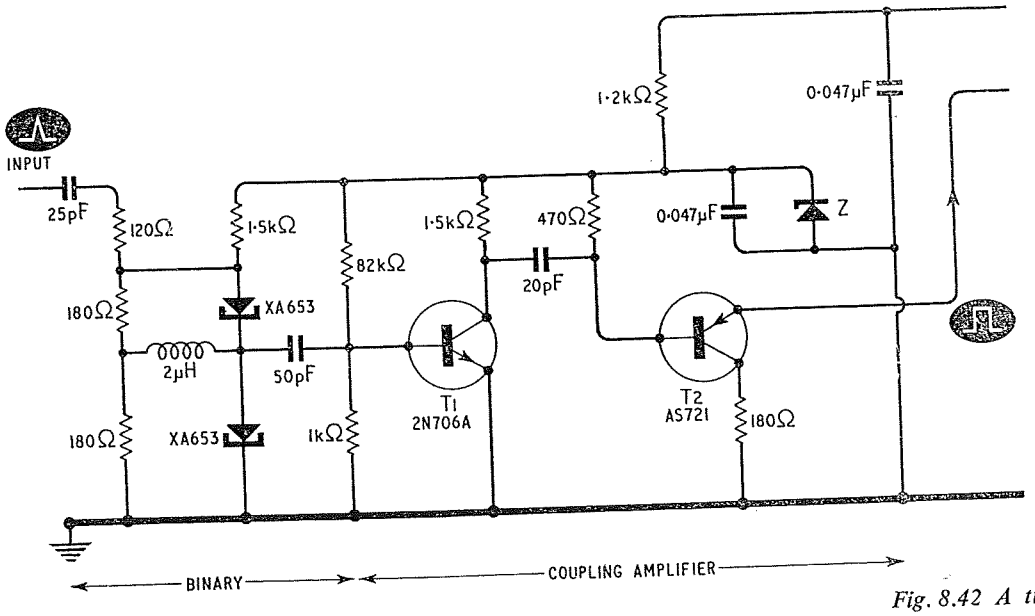


Fig. 8.42 A tunnel

The double pulse resolving time is less than 14×10^{-9} sec, but the resetting operation takes about 50×10^{-9} sec. Two transistors are used in the reset circuit.

Rabinovici has designed a decade counter using only four tunnel diodes in a decimal coded binary system[49]. The tunnel diodes used must have parameters which satisfy certain relationships if the ten stable states are to be obtained using only four diodes.

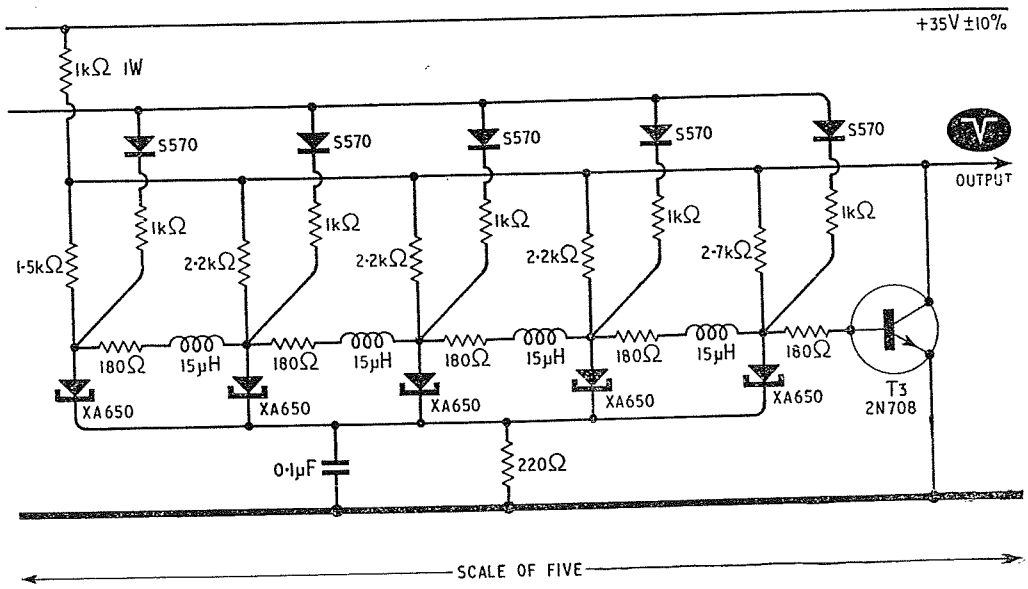
8.3.3 Ring-like circuits

Few tunnel diode ring circuits have been published up to the present time. A five stage ring-like circuit which uses germanium tunnel diodes and consumes only about 10 mW of power is shown in Fig. 8.41[45]. The maximum frequency of operation of this circuit is limited to about 0.5 Mc/s by the characteristics of the transistors used.

Initially all of the tunnel diodes are in their low voltage states. A negative going input pulse will switch TD_1 only to the high voltage state because this diode is receiving a larger bias current than the other diodes owing to the smaller value of its load resistor. The potential of the cathode of TD_1 becomes more negative and the transistor $T1$ is switched into the conducting state. The next input pulse can switch TD_2 into its high voltage state, since this diode is now biased by the current passing through $T1$. Hence $T2$ is switched to conduction and the third input pulse can switch TD_3. When TD_5 is switched by the fifth input pulse to its high voltage state, $T5$ conducts and virtually shorts all of the tunnel diodes to earth. They therefore return to the low voltage state and the circuit has been reset to zero.

This circuit differs from the conventional ring counter in that the diodes which have been switched remain in their high voltage state until the whole circuit is reset. Negative going input pulses of 3 V amplitude are required. The output pulses are positive going and of the same amplitude.

A 20 Mc/s decade scaler is shown in Fig. 8.42[45]. The circuit comprises a binary employing two XA653 gallium arsenide 5 mA tunnel diodes followed by a five stage counter using XA650 Texas Instruments gallium arsenide tunnel diodes. The functioning of the scale of five circuit is similar to that of Fig. 8.41, but the tunnel diode connections have been inverted for operation from a positive power supply and positive going input pulses. Coupling transistors are not required in the scale of five, but an NPN 2N708 transistor, $T3$, is usedto reset it. $T1$ and $T2$ are coupling amplifiers, $T2$ being connected as an emitter follower to provide the low



diode decade circuit

impedance output which can operate the scale of five. The input pulses should be positive going and of amplitude 0.4 V, whilst the output pulses are negative going of amplitude 6 V.

8.4 CIRCUITS USING MAGNETIC OR FERRO-ELECTRIC MATERIALS WITH RECTANGULAR HYSTERESIS LOOPS

Magnetic materials can be produced which have a hysteresis loop which is approximately rectangular in shape as shown in Fig. 8.43. If a coil is wound around a toroid of such material, the direction of magnetisation may be switched from $-B_{sat}$ to

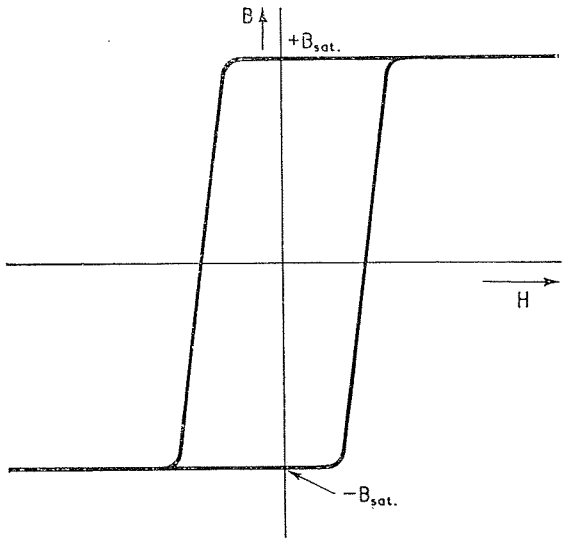


Fig. 8.43 A rectangular hysteresis loop

$+B_{sat}$ by passing a suitable current pulse through the coil. A current pulse of the opposite polarity will return the toroid to its initial state. Binary and ring counters can be constructed using this type of bistable circuit.

If the current pulses applied to a magnetic core have a duration which is smaller than the time required for the direction of magnetisation of the core to be reversed, the state of the core will change only a part of the way from $-B_{sat}$ to $+B_{sat}$. A number of pulses must therefore be applied to the circuit before the direction of magnetisation is completely reversed and several stable intermediate states can thus be created. Scaling circuits which use these states of increasing flux for counting are known as flux counters.

Magnetic cores have been widely used as memory devices in computers and can retain information even if the power supply to the apparatus is switched off, but up to the present time they have not been

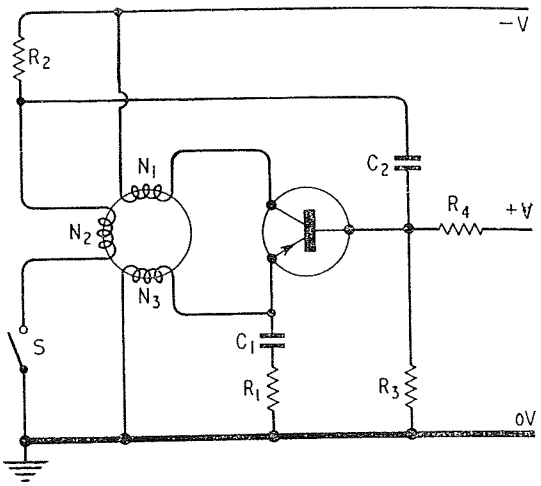


Fig. 8.44 A simple flux counter

used very frequently for pure counting. This is partly due to the difficulty of arranging readout systems for magnetic core counters. Magnetic core counters do, however, have the advantages that they require relatively few components, normally consume negligible power during quiescent periods and are very small and reliable. They are very suitable for use in space vehicles[50].

Transistors are very suitable for controlling the current pulses to magnetic cores, since their low output impedance can easily be matched to the impedance of the core winding. Normally the transistors are used in a blocking oscillator circuit, the magnetic material being used as the transformer core. The circuits require rather careful design[51].

Relatively simple decade counters, such as that shown in Fig. 8.44, can be designed using magnetic cores[52]. S is an electronic switch which generates the input pulses. Each current pulse must be so short that it causes only a partial reversal of the direction of magnetisation as it flows through N_2 and R_2. If the operating point on the hysteresis loop

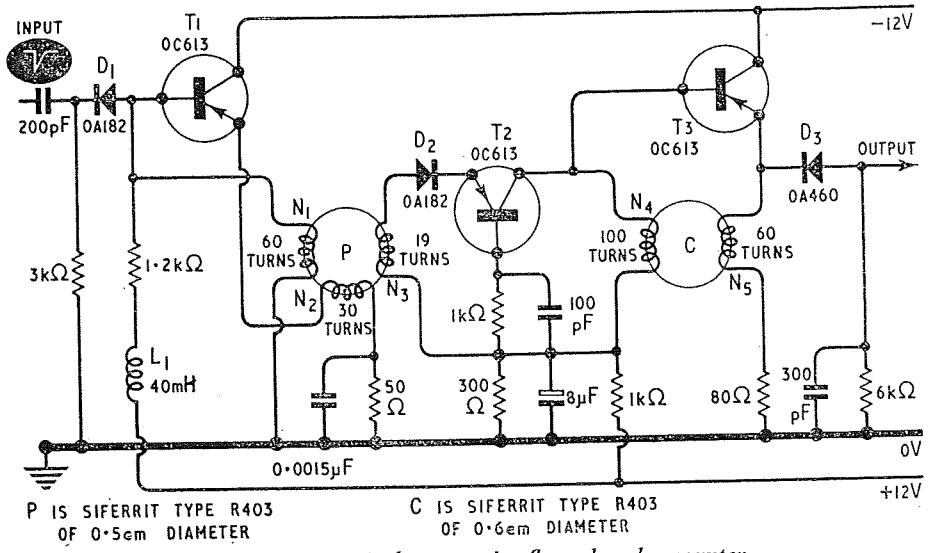


Fig. 8.45 A practical magnetic flux decade counter

is initially at $-B_{sat}$, successive input pulses will cause it to move by degrees to $+B_{sat}$. The coil inductance has now decreased, since a further input pulse can cause little increase in the magnetic induction. Once saturation has been reached, almost all of the input voltage of the next pulse will appear across R_2 instead of across N_2. The pulse from R_2 is differentiated by C_2-R_3 and is used to switch the transistor to conduction. A current passes through N_1 and the operating point is returned to $-B_{sat}$. Although this circuit will function reliably, it is only satisfactory over a temperature range of about 4 °C, since the magnetic properties of the core are very temperature dependent.

In order to construct a magnetic counter which can be operated over a reasonably wide temperature range, it is almost essential to employ two cores which have very similar temperature dependencies[52]. In one type of circuit the input pulses are fed to a 'pumping' core which is taken through a complete magnetic cycle for each input pulse applied to the circuit. A winding on the pumping core supplies pulses to a coupling circuit which operates the second core which is known as the counting core. Each input pulse only partly reverses the direction of magnetisation of the counting core, but after a number of pulses have been applied the core becomes saturated in the opposite direction to its initial state; it is then returned to its zero state.

A practical counter circuit based on this principle is shown in Fig. 8.45; two blocking oscillators are used[52]. A bias current passes through N_1 and the 1.2 kΩ resistor. This current is capable of returning the pumping core, P, to its quiescent state. A negative going input pulse will trigger the first blocking oscillator and the direction of magnetisation of the core P is momentarily reversed. The output from P supplied by N_3 is amplified by $T2$ and is used to partly change the state of the counting core, C. When C becomes saturated, the transistor $T3$ is triggered by the difference in voltage between N_4 and N_5. $T3$ is normally cut off by the positive potential applied to its base.

The maximum frequency of operation of the circuit shown is about 128 kc/s and is limited by the rapidity with which the cores return to their quiescent state. If L_1 is omitted the pumping core takes longer to return to its quiescent state and the maximum frequency is limited to about 40 kc/s. The operation of the circuit is almost independent of temperature. The scale in which the circuit counts can be altered by varying the number of turns on the core windings or by varying the values of the resistors in the coupling circuit. The counting capacity may be changed very conveniently, however, by bringing a small permanent magnet near to the pumping core to increase the capacity or near to the counting core to reduce the capacity. The

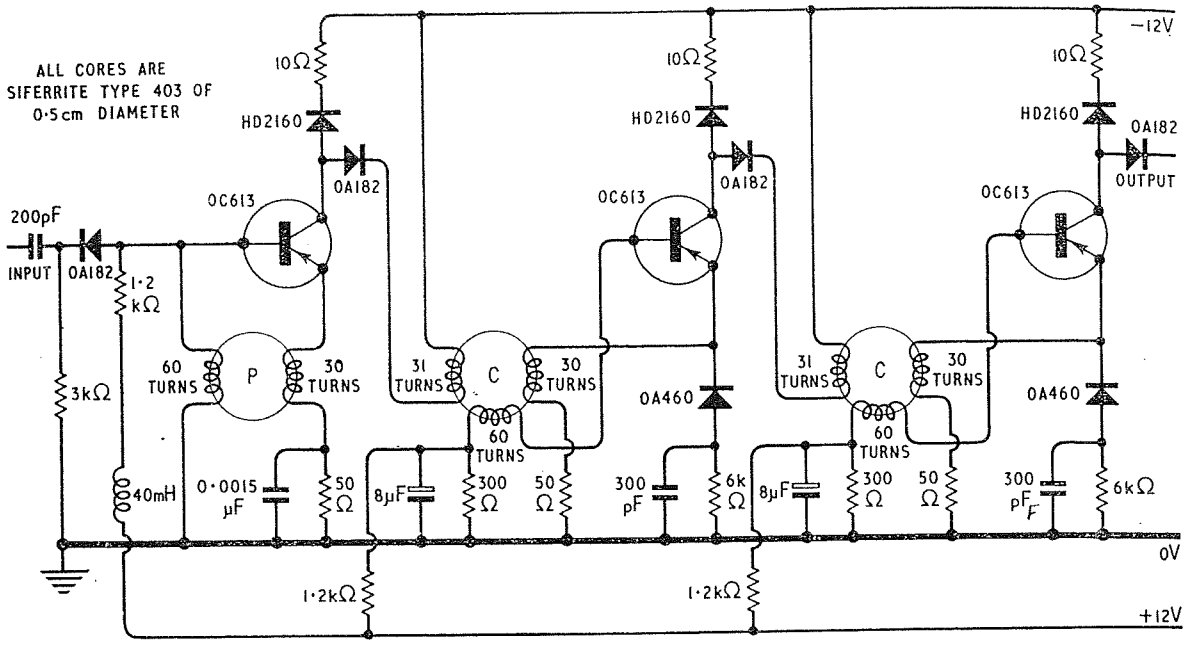


Fig. 8.46 A two decade magnetic flux counter

count capacity may easily be varied from 6 to 16 by this method[52]. It is necessary to have some control over the count capacity to overcome the effects of component tolerances.

It is not essential to use two cores in any decade after the first, since the counting core of the first decade yields a temperature dependent signal and acts as a pumping core for the next decade. A two decade counter employing only three magnetic cores is shown in Fig. 8.46[52]. A simplified method of coupling is employed in this circuit so that only one transistor is required in any decade after the first.

These circuits are excellent frequency dividers, but the problem of providing a method of readout for them is a difficult one, since the information on the state of the count is contained in the magnetic flux of the cores. There is no known method of providing readout without interfering with the counting process. If the decades are separated from each other by gates, at the end of the counting process the number of additional pulses from a pulse source required to bring about saturation in each of the cores may be found; this is the complement of the number counted. In an alternative method of readout, the decades are again separated by gates and ten pulses are applied to each decade; the number of pulses arriving at each decade after that decade has saturated are counted on a separate instrument.

A number of other flux counter circuits have been published[50, 53–55] in addition to full details of the principles of operation[56].

8.4.1 Magnetic Readout

An interesting ring type of decade scaling system with magnetic readout has been developed at Harwell[57–58]. Basically this system consists of ten rod like magnetic cores placed in a circle with their longtitudinal axes perpendicular to the plane of the circle. They have rectangular hysteresis loops. A pivoted spindle passes through the centre of the cylindrical arrangement and two compass needles are connected astatically at each end of the spindle. At any one time nine of the cores are magnetised longtitudinally in one direction, whilst the tenth core is magnetised in the opposite direction. Each input pulse causes two cores to be switched so that another core is now magnetised in the opposite

direction to the other nine cores. The pattern of magnetisation is thus rotated one place by each input pulse. One pole of each of the compass needles is attracted by the core which is magnetised in the opposite direction to the others and is repelled by the other nine cores. The compass needles, therefore, follow the rotation of the magnetic pattern at low counting speeds, but at high speeds they will come to rest at the correct place a very short time after the counting has ceased. A pointer attached to the spindle to which the compass needles are fixed shows the state of the count; it will continue to do this even after the power supply has been cut off. The resolving time of the system can be made less then 1 μsec. In the quiescent state the only power consumed is about 100 μW per decade (at 20 °C) to supply the transistor leakage current. An additional power of about 3.5 μW per count per second is required when counting is taking place. A 15 V power supply is used.

The spindle is mounted in jewelled pivots of the type used in microammeters. It is operated in oil, the viscosity of which is chosen to give a suitable mechanical damping. Decades constructed on these principles have been made in cylinders $2\frac{3}{16}$ in. diameter and 6 in. long. The front face houses the indicator needle which may be compared with the hand of a watch. The face is marked with the digits 0 to 9.

In the later version the cores consist of films of nickel-iron alloy deposited electrolytically on 13 s.w.g. copper rods. It is necessary to apply a magnetic field during the deposition in order to produce a preferred direction of magnetisation which results in a rectangular hysteresis loop. The magnetic films have a thickness of 1.8×10^{-4} cm.

The cores are driven by XA112 transistors used in a type of blocking oscillator circuit. Each transistor switches two of the cores once during the time ten input pulses are applied to the decade. An input pulse triggers only the transistor whose core is magnetised in the opposite direction to that of the other cores. The transistor conducts until the core is magnetised in the same direction as the others and also provides a pulse which switches the succeeding core. Inter-decade coupling circuits using one transistor and one core with a rectangular hysteresis loop are used. The same circuit can be employed to trigger the first decade at input frequencies up to 100 kc/s, but at higher frequencies a bistable input circuit is used.

8.4.2 Circuits Using Ferro-electric Capacitors

Ferro-electric materials can be considered to be the electrical analogues of ferro-magnetic substances and are used as the dielectric in capacitors. If the polarisation of such a capacitor is plotted (on the vertical axis) against the potential applied across the capacitor, a rectangular hysteresis loop similar to the magnetic hysteresis loop of Fig. 8.43 can be obtained[59]. Thus when a voltage pulse is applied to a ferro-electric capacitor, the capacitor does not return to its initial state at the end of the pulse.

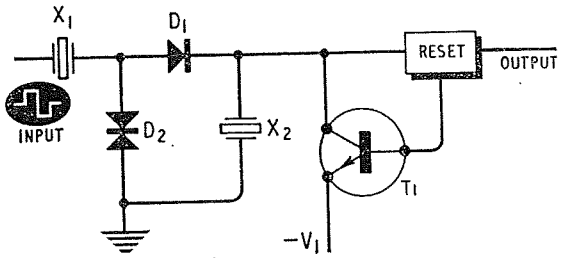


Fig. 8.47 A counting circuit employing ferro-electric devices

The displaced charge can remain in the dielectric for a long time, but readout difficulties similar to those encountered with magnetic counters arise.

The ferro-electric crystals, like ferro-magnetic materials, contain domains and there is a Curie temperature above which the ferro-electric properties disappear. Possibly the most useful ferro-electric material is barium titanate, but a number of others such as potassium niobate and guanidine aluminium sulphate hexahydrate are known.

If a potential is applied to a ferro-electric capacitor, the device behaves more or less as a small resistor in series with a fixed potential. As soon as it is completely polarised, however, it behaves as a capacitor of very small value.

The basic type of counter in which ferro-electric capacitors may be used is shown in Fig. 8.47[60]. When the positive part of the input pulse is applied to the circuit, the ferro-electric capacitor X_1 has

its direction of polarisation completely reversed and the charge which passes through it also passes through D_1 to the ferro-electric capacitor X_2. The charge passed to X_2 is almost independent of the size of the input pulse provided that this exceeds a certain minimum value, since once X_1 has completely switched it behaves as a very small capacitor and an increase in the input pulse voltage will not appreciably increase the charge passed to X_2. X_2 is several times larger than X_1 and its polarisation will therefore only be partly reversed by the charge from X_1. The negative going part of the input pulse returns X_1 to the zero state, the current passing through the double anode breakdown diode D_2 which is equivalent to two silicon diodes mounted back to back.

The next input pulse will switch X_1 again and cause the same charge to be fed to X_2 as before. After a number of input pulses X_2 will saturate (become fully polarised) and a further input pulse will now cause the voltage across X_2 to increase considerably. The reset circuit is thus triggered and a positive pulse is fed to the base of the NPN transistor $T1$. The transistor conducts and the negative voltage $-V_1$ is applied to the upper end of X_2 which is thus switched to its initial state of polarisation.

If X_2 is ten times the size of X_1, a decade counter is formed. This type of circuit has been used for counting in scales of up to 40. The switching time is small and the pulse spacing may range from a few microseconds to some days. The maximum counting frequency is limited by the heat dissipation in X_1.

Similar types of circuit have been proposed[61] in which ordinary capacitors are used for X_1 and X_2, but such circuits have several disadvantages. The charge passed from X_1 to X_2 is not independent of the input pulse voltage, the counting capacity must be fairly small and the pulse spacing should not exceed about 5 msec owing to leakage of charge from X_2.

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